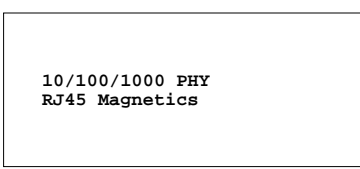
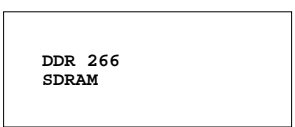
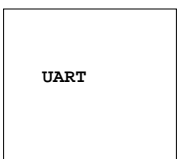
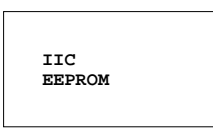
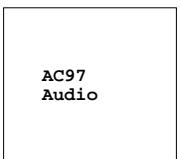
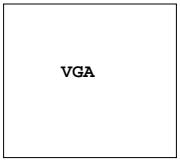
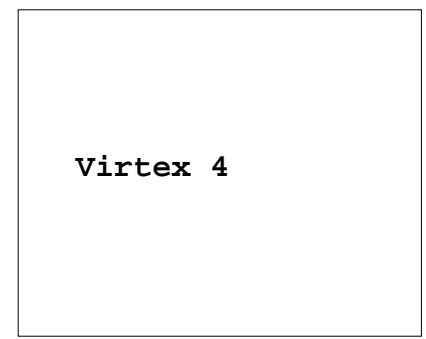
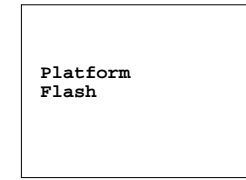
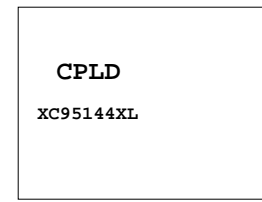
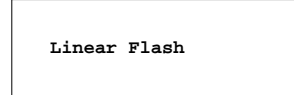
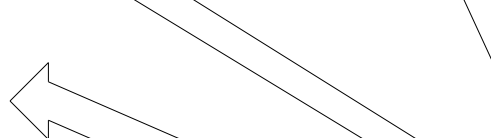
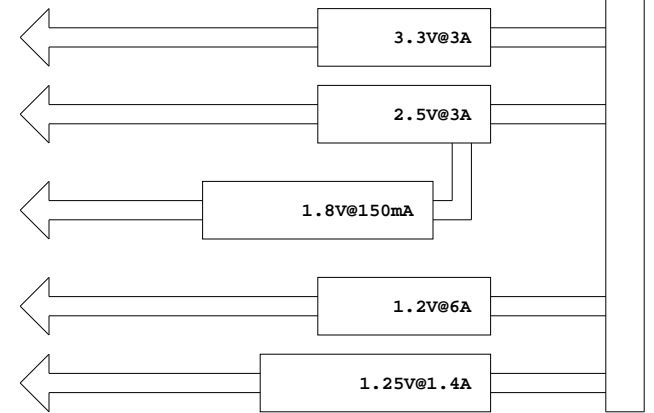
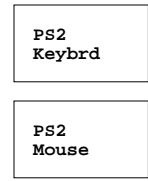
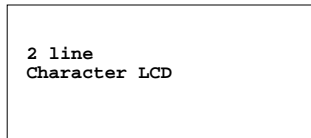
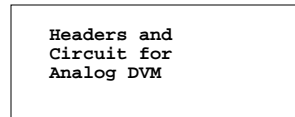
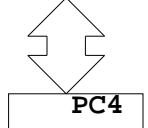
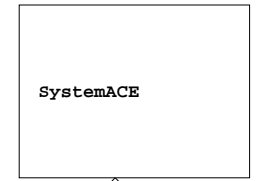
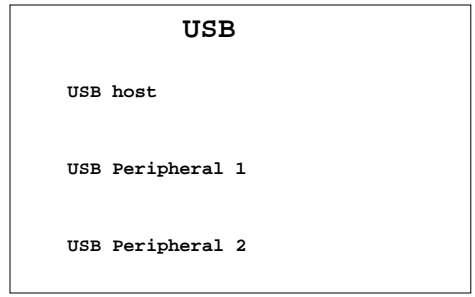


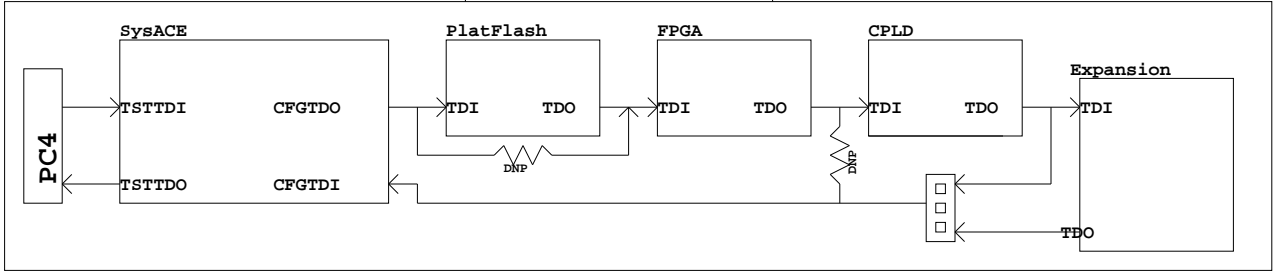
Power Supply



Compatibility and Available IOs	
FPGA Device	Banks
LX15, FX12, SX25	8 Banks 320 User IOs
LX25, LX40, LX60 SX35	10 Banks up to 448 User IOs



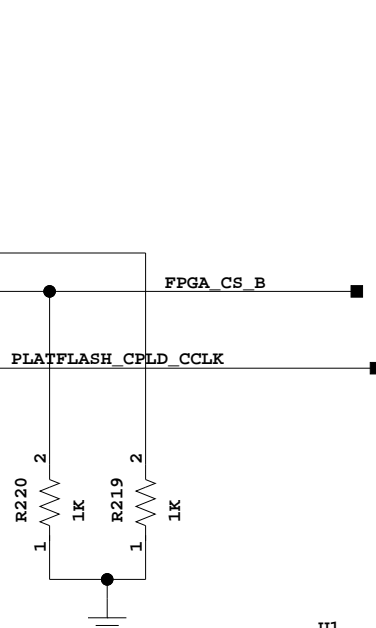
JTAG Chain



Title: ML401/2/3 Block Diagram	
Date: 8/19/2004	Ver: 1.0
Sheet Size: B	Rev: B
Sheet 1 of 24	Drawn By BF

TDP_0_H13
 TDN_0_G13
 TDI_0_Y12
 DOUT_BUSY_0_Y14
 M1_0_Y15
 TCK_0_W12
 TDO_0_Y13
 M0_0_W15
 TMS_0_Y11
 PWRDWN_B_0_W13
 M2_0_W14
 VBATT_0_Y16
 RDWR_B_0_H12
 DONE_0_H14
 CS_B_0_G11
 INIT_0_G15
 PROGRAM_B_0_H15
 D_IN_0_G12
 CCLK_0_G14
 HSWAPEN_0_G16

H13 NC
 G13 NC
 Y12 FPGA_TDI
 Y14 FPGA_DOUT_BUSY
 Y15 FPGA_M1
 W12 FPGA_PROM_CPLD_TCK
 Y13 FPGA_TDO
 W15 FPGA_M0
 Y11 FPGA_PROM_CPLD_TMS
 W13 NC
 W14 FPGA_M2
 Y16 FPGA_VBATT
 H12
 H14 FPGA_DONE
 G11
 G15 FPGA_INIT
 H15 FPGA_PROG_B
 G12 FPGA_DIN
 G14 FPGA_CCLK
 G16



Added 50ohm for protection
 In case FPGA and PLAT Flash
 or CPLD drive CCLK

FPGA_BANK0
 3.3V VCC0
 Configuration

IO_L8N_D16_CC_LC_1_D12
 IO_L8P_D17_CC_LC_1_E13
 IO_L7N_D18_LC_1_C16
 IO_L7P_D19_LC_1_D16
 IO_L6N_D20_LC_1_D11
 IO_L6P_D21_LC_1_C11
 IO_L5N_D22_LC_1_E14
 IO_L5P_D23_LC_1_D15
 IO_L4N_D24_VREF_LC_1_D13
 IO_L4P_D25_LC_1_D14
 IO_L3N_D26_LC_1_F15
 IO_L3P_D27_LC_1_F16
 IO_L2N_D28_LC_1_F11
 IO_L2P_D29_LC_1_F12
 IO_L1N_D30_LC_1_F13
 IO_L1P_D31_LC_1_F14
 VP_SM_AF16
 VN_SM_AF15

D12 SRAM_FLASH_D16
 E13 SRAM_FLASH_D17
 C16 SRAM_FLASH_D18
 D16 SRAM_FLASH_D19
 D11 SRAM_FLASH_D20
 C11 SRAM_FLASH_D21
 E14 SRAM_FLASH_D22
 D15 SRAM_FLASH_D23
 D13 SRAM_FLASH_D24
 D14 SRAM_FLASH_D25
 F15 SRAM_FLASH_D26
 F16 SRAM_FLASH_D27
 F11 SRAM_FLASH_D28
 F12 SRAM_FLASH_D29
 F13 SRAM_FLASH_D30
 F14 SRAM_FLASH_D31
 AF16 SYS_MON_VP0
 AF15 SYS_MON_VN0

FPGA_BANK1
 3.3V VCC0

IO_L8N_D0_LC_2_AD13
 IO_L8P_D1_LC_2_AC13
 IO_L7N_D2_LC_2_AC15
 IO_L7P_D3_LC_2_AC16
 IO_L6N_D4_LC_2_AA11
 IO_L6P_D5_LC_2_AA12
 IO_L5N_D6_LC_2_AD14
 IO_L5P_D7_LC_2_AC14
 IO_L4N_D8_VREF_LC_2_AA13
 IO_L4P_D9_LC_2_AB13
 IO_L3N_D10_LC_2_AA15
 IO_L3P_D11_LC_2_AA16
 IO_L2N_D12_LC_2_AC11
 IO_L2P_D13_LC_2_AC12
 IO_L1N_D14_CC_LC_2_AB14
 IO_L1P_D15_CC_LC_2_AA14

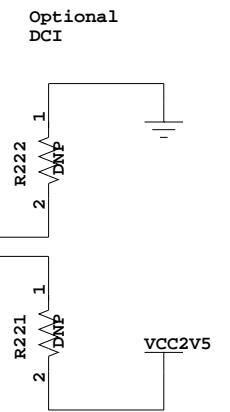
AD13 SRAM_FLASH_D0
 AC13 SRAM_FLASH_D1
 AC15 SRAM_FLASH_D2
 AC16 SRAM_FLASH_D3
 AA11 SRAM_FLASH_D4
 AA12 SRAM_FLASH_D5
 AD14 SRAM_FLASH_D6
 AC14 SRAM_FLASH_D7
 AA13 SRAM_FLASH_D8
 AB13 SRAM_FLASH_D9
 AA15 SRAM_FLASH_D10
 AA16 SRAM_FLASH_D11
 AC11 SRAM_FLASH_D12
 AC12 SRAM_FLASH_D13
 AB14 SRAM_FLASH_D14
 AA14 SRAM_FLASH_D15

FPGA_BANK2
 3.3V VCC0

IO_L8N_GC_LC_3_C12
 IO_L8P_GC_LC_3_C13
 IO_L7N_GC_LC_3_A17
 IO_L7P_GC_LC_3_B17
 IO_L6N_GC_LC_3_B10
 IO_L6P_GC_LC_3_A10
 IO_L5N_GC_LC_3_A15
 IO_L5P_GC_LC_3_A16
 IO_L4N_GC_VREF_LC_3_B12
 IO_L4P_GC_LC_3_B13
 IO_L3N_GC_LC_3_C14
 IO_L3P_GC_LC_3_C15
 IO_L2N_GC_VRP_LC_3_A11
 IO_L2P_GC_VRN_LC_3_A12
 IO_L1N_GC_CC_LC_3_B14
 IO_L1P_GC_CC_LC_3_B15

C12 SMA_DIFF_CLK_IN_N
 C13 SMA_DIFF_CLK_IN_P
 A17 IIC_SCL
 B17 IIC_SDA
 B10 DDR_CK1_N
 A10 DDR_CK1_P
 A15 DDR_A13
 A16 DDR_BA1
 B12 DDR_BA0
 B13 DDR_CK1_P (Feedback)
 C14 MOUSE_DATA
 C15 PHY_TXCLK
 A11 GPIO_LED_2
 A12 GPIO_LED_3
 B14 MOUSE_CLK
 B15 PHY_RXC_RXCLK

FPGA_BANK3
 2.5V VCC0



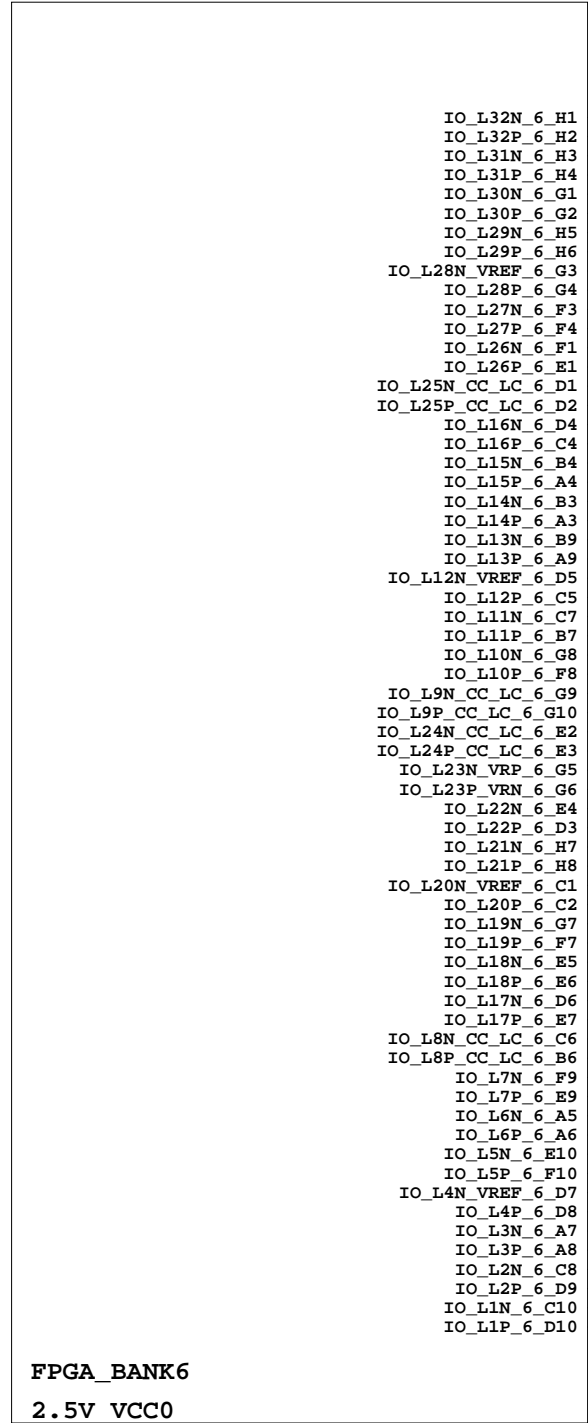
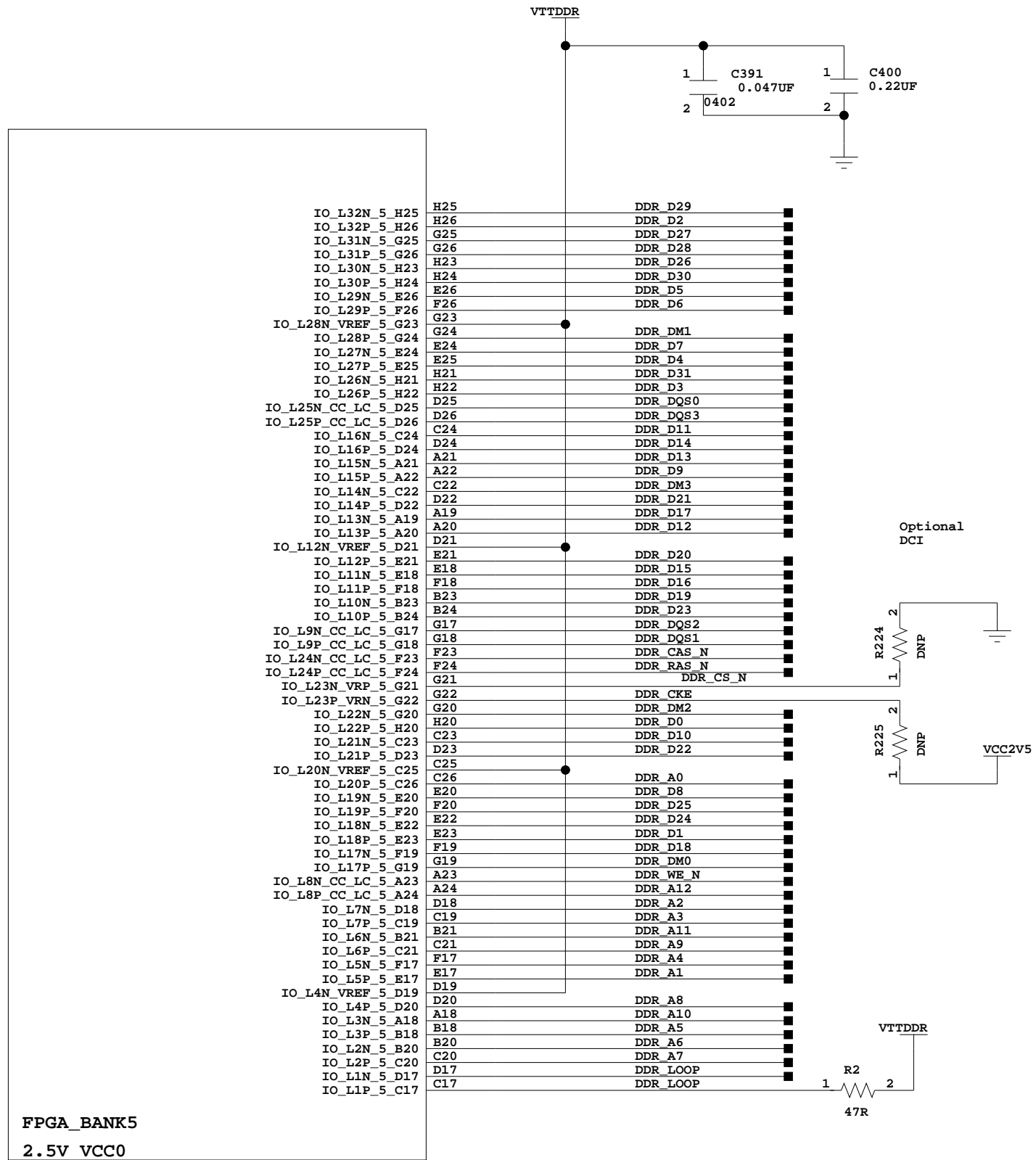
IO_L8N_GC_CC_LC_4_AD11
 IO_L8P_GC_CC_LC_4_AD12
 IO_L7N_GC_VRP_LC_4_AD16
 IO_L7P_GC_VRN_LC_4_AD17
 IO_L6N_GC_LC_4_AD10
 IO_L6P_GC_LC_4_AE10
 IO_L5N_GC_LC_4_AE13
 IO_L5P_GC_LC_4_AE14
 IO_L4N_GC_VREF_LC_4_AF10
 IO_L4P_GC_LC_4_AF11
 IO_L3N_GC_LC_4_AC17
 IO_L3P_GC_LC_4_AB17
 IO_L2N_GC_LC_4_AB10
 IO_L2P_GC_LC_4_AC10
 IO_L1N_GC_LC_4_AE12
 IO_L1P_GC_LC_4_AF12

AD11 FPGA_DIN (Feedback)
 AD12 USERCLK
 AD16 AUDIO_SDATA_IN
 AD17 SRAM_CLK (Feedback)
 AD10 FLASH_AUDIO_RESET_N
 AE10 AUDIO_BIT_CLK
 AE13 LCD_E
 AE14 SYSCLK_100MHZ
 AF10 USB_CS_N
 AF11 SYSACE_CLK
 AC17 LCD_RS
 AB17 LCD_RW
 AB10 LCD_DB4
 AC10 LCD_DB5
 AE12 LCD_DB6
 AF12 LCD_DB7

FPGA_BANK4
 3.3V VCC0



Title: FPGA Banks 0,1,2,3,4	
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 2 of 24	Drawn By BF



XILINX

Title:
FPGA Bank 5, 6

Date: _____ Ver: _____

Sheet Size: B Rev: B

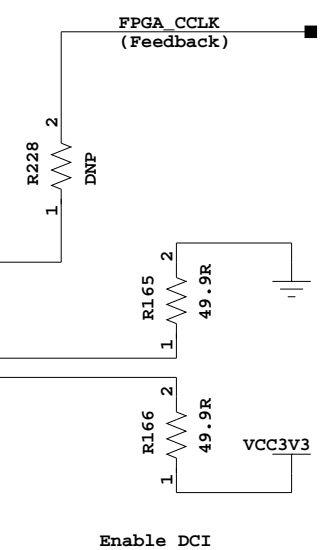
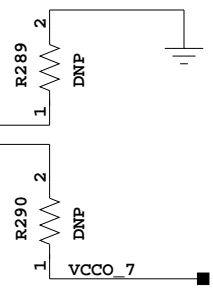
Sheet 3 of 24 Drawn By BF

IO_L16N_7_AC24	AC24	HDR1_2
IO_L16P_7_AC23	AC23	HDR1_4
IO_L15N_7_AD23	AD23	HDR1_6
IO_L15P_7_AD22	AD22	HDR1_8
IO_L14N_7_AA23	AA23	HDR1_10
IO_L14P_7_AB23	AB23	HDR1_12
IO_L13N_7_AB22	AB22	HDR1_14
IO_L13P_7_AC22	AC22	HDR1_16
IO_L12N_VREF_7_Y23	Y23	HDR2_6
IO_L12P_7_Y22	Y22	HDR2_8
IO_L11N_7_AD26	AD26	HDR1_18
IO_L11P_7_AD25	AD25	HDR1_20
IO_L10N_7_AA26	AA26	HDR1_22
IO_L10P_7_AB26	AB26	HDR1_24
IO_L9N_CC_LC_7_AC26	AC26	HDR1_34
IO_L9P_CC_LC_7_AC25	AC25	HDR1_36
IO_L8N_CC_LC_7_Y24	Y24	HDR1_26
IO_L8P_CC_LC_7_AA24	AA24	HDR1_28
IO_L7N_7_AB25	AB25	HDR1_30
IO_L7P_7_AB24	AB24	HDR1_32
IO_L6N_7_Y26	Y26	HDR1_38
IO_L6P_7_Y25	Y25	HDR1_40
IO_L5N_7_V20	V20	HDR1_42
IO_L5P_7_W20	W20	HDR1_44
IO_L4N_VREF_7_W24	W24	HDR2_10
IO_L4P_7_W23	W23	HDR2_12
IO_L3N_7_W22	W22	HDR1_46
IO_L3P_7_W21	W21	HDR1_48
IO_L2N_7_W26	W26	HDR1_50
IO_L2P_7_W25	W25	HDR1_52
IO_L1N_7_V22	V22	HDR1_54
IO_L1P_7_V21	V21	HDR1_56
IO_L24N_CC_LC_7_AB21	AB21	HDR1_58
IO_L24P_CC_LC_7_AC21	AC21	HDR1_60
IO_L23N_VRP_7_AD20	AD20	HDR2_14
IO_L23P_VRN_7_AE20	AE20	HDR2_16
IO_L22N_7_AE24	AE24	HDR1_62
IO_L22P_7_AF24	AF24	HDR1_64
IO_L21N_7_Y18	Y18	HDR2_2
IO_L21P_7_AA18	AA18	HDR2_4
IO_L20N_VREF_7_Y21	Y21	HDR2_18
IO_L20P_7_Y20	Y20	HDR2_20
IO_L19N_7_AE23	AE23	HDR2_22
IO_L19P_7_AF23	AF23	HDR2_24
IO_L18N_7_W19	W19	HDR2_26
IO_L18P_7_Y19	Y19	HDR2_28
IO_L17N_7_AF20	AF20	HDR2_30
IO_L17P_7_AF19	AF19	HDR2_32
IO_L32N_SM7_7_AD21	AD21	HDR2_34 SYS MON VN7
IO_L32P_SM7_7_AE21	AE21	HDR2_36 SYS MON VP7
IO_L31N_SM6_7_AE18	AE18	HDR2_38 SYS MON VN6
IO_L31P_SM6_7_AF18	AF18	HDR2_40 SYS MON VP6
IO_L30N_SM5_7_AF22	AF22	HDR2_42 SYS MON VN5
IO_L30P_SM5_7_AF21	AF21	HDR2_44 SYS MON VP5
IO_L29N_SM4_7_AB18	AB18	HDR2_46 SYS MON VN4
IO_L29P_SM4_7_AC18	AC18	HDR2_48 SYS MON VP4
IO_L28N_VREF_7_AC20	AC20	HDR2_50
IO_L28P_7_AB20	AB20	HDR2_52
IO_L27N_SM3_7_AA17	AA17	HDR2_54 SYS MON VN3
IO_L27P_SM3_7_Y17	Y17	HDR2_56 SYS MON VP3
IO_L26N_SM2_7_AA20	AA20	HDR2_58 SYS MON VN2
IO_L26P_SM2_7_AA19	AA19	HDR2_60 SYS MON VP2
IO_L25N_CC_SM1_LC_7_AC19	AC19	HDR2_62 SYS MON VN1
IO_L25P_CC_SM1_LC_7_AD19	AD19	HDR2_64 SYS MON VP1

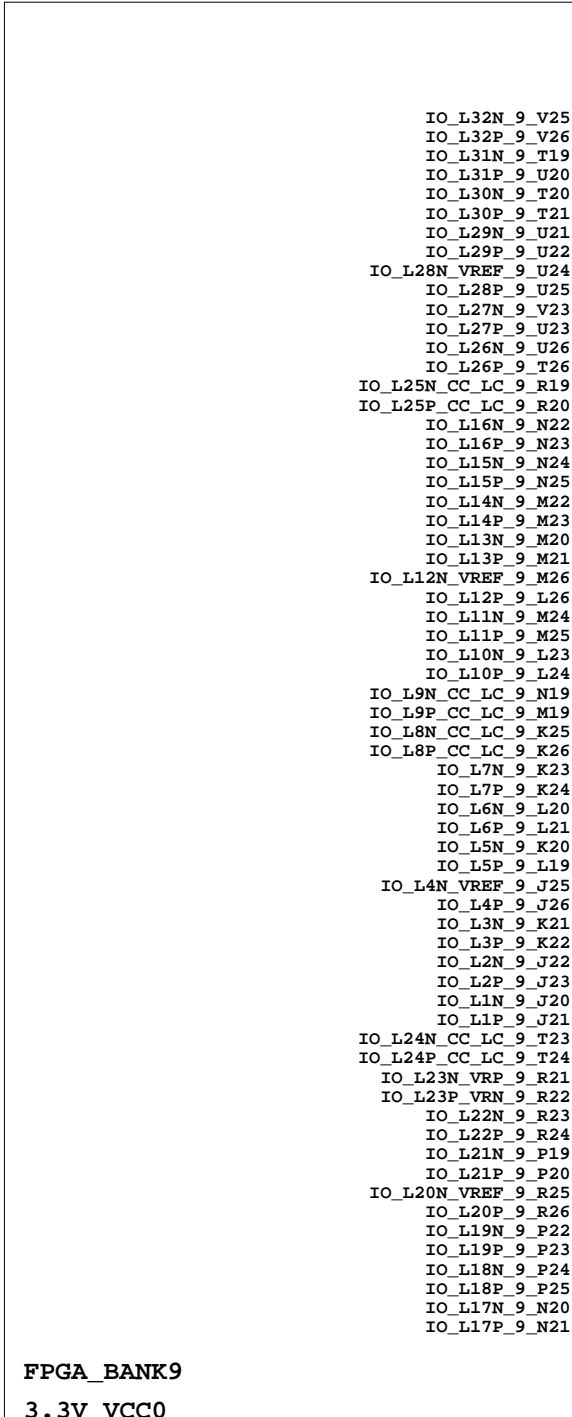
FPGA_BANK7
3.3V or 2.5V VCC0

IO_L16N_8_AD1	AD1	SRAM FLASH A7
IO_L16P_8_AD2	AD2	SRAM FLASH A8
IO_L15N_8_AE3	AE3	SRAM FLASH A9
IO_L15P_8_AF3	AF3	SRAM FLASH A10
IO_L14N_8_AC1	AC1	SRAM FLASH A5
IO_L14P_8_AC2	AC2	SRAM FLASH A6
IO_L13N_8_AB5	AB5	SRAM FLASH A19
IO_L13P_8_AC5	AC5	SRAM FLASH A20
IO_L12N_VREF_8_AB2	AB2	SRAM FLASH A4
IO_L12P_8_AB3	AB3	SRAM FLASH A16
IO_L11N_8_AB4	AB4	SRAM FLASH A17
IO_L11P_8_AC4	AC4	SRAM FLASH A18
IO_L10N_8_AA1	AA1	SRAM FLASH A2
IO_L10P_8_AB1	AB1	SRAM FLASH A3
IO_L9N_CC_LC_8_Y5	Y5	SRAM BW1
IO_L9P_CC_LC_8_Y6	Y6	SRAM BW0
IO_L8N_CC_LC_8_Y3	Y3	SRAM BW3
IO_L8P_CC_LC_8_Y4	Y4	SRAM BW2
IO_L7N_8_AA3	AA3	SRAM FLASH A14
IO_L7P_8_AA4	AA4	SRAM FLASH A15
IO_L6N_8_Y1	Y1	SRAM FLASH A0
IO_L6P_8_Y2	Y2	SRAM FLASH A1
IO_L5N_8_W5	W5	SRAM FLASH A13
IO_L5P_8_W6	W6	SRAM FLASH A12
IO_L4N_VREF_8_W3	W3	SRAM FLASH A11
IO_L4P_8_W4	W4	SRAM ADV LD N
IO_L3N_8_V7	V7	SRAM CE1 N
IO_L3P_8_W7	W7	FLASH CE2
IO_L2N_8_V5	V5	USB INT
IO_L2P_8_V6	V6	BUS ERROR 1
IO_L1N_8_W1	W1	UART SOUT
IO_L1P_8_W2	W2	UART SIN
IO_L24N_CC_LC_8_AB6	AB6	SRAM FLASH WE N
IO_L24P_CC_LC_8_AC6	AC6	SRAM FLASH OE N
IO_L23N_VRP_8_AD7	AD7	
IO_L23P_VRN_8_AE7	AE7	
IO_L22N_8_AD4	AD4	SYSACE MPIRQ
IO_L22P_8_AD5	AD5	SYSACE MPCE
IO_L21N_8_Y9	Y9	SYSACE MPA06
IO_L21P_8_AA9	AA9	SYSACE MPA05
IO_L20N_VREF_8_Y7	Y7	SYSACE MPA04
IO_L20P_8_AA7	AA7	SYSACE USB D15
IO_L19N_8_AF5	AF5	SYSACE USB D14
IO_L19P_8_AF6	AF6	SYSACE USB D13
IO_L18N_8_AC3	AC3	SYSACE USB D12
IO_L18P_8_AD3	AD3	SYSACE USB D11
IO_L17N_8_AE4	AE4	SYSACE USB D10
IO_L17P_8_AF4	AF4	SYSACE USB D9
IO_L32N_8_AC8	AC8	SYSACE USB D8
IO_L32P_8_AD8	AD8	SYSACE USB D7
IO_L31N_8_AE9	AE9	SYSACE USB D6
IO_L31P_8_AF9	AF9	SYSACE USB D5
IO_L30N_8_AD6	AD6	SYSACE USB D4
IO_L30P_8_AE6	AE6	SYSACE USB D3
IO_L29N_8_AB9	AB9	SYSACE USB D2
IO_L29P_8_AC9	AC9	SYSACE USB D1
IO_L28N_VREF_8_AB7	AB7	SYSACE USB D0
IO_L28P_8_AC7	AC7	SYSACE MPA03
IO_L27N_8_AA10	AA10	SYSACE A2 USB A1
IO_L27P_8_Y10	Y10	SYSACE A1 USB A0
IO_L26N_8_Y8	Y8	SYSACE MPWE USB WR N
IO_L26P_8_AA8	AA8	SYSACE MPOE USB RD N
IO_L25N_CC_LC_8_AF7	AF7	SRAM CLK
IO_L25P_CC_LC_8_AF8	AF8	VGA CLK

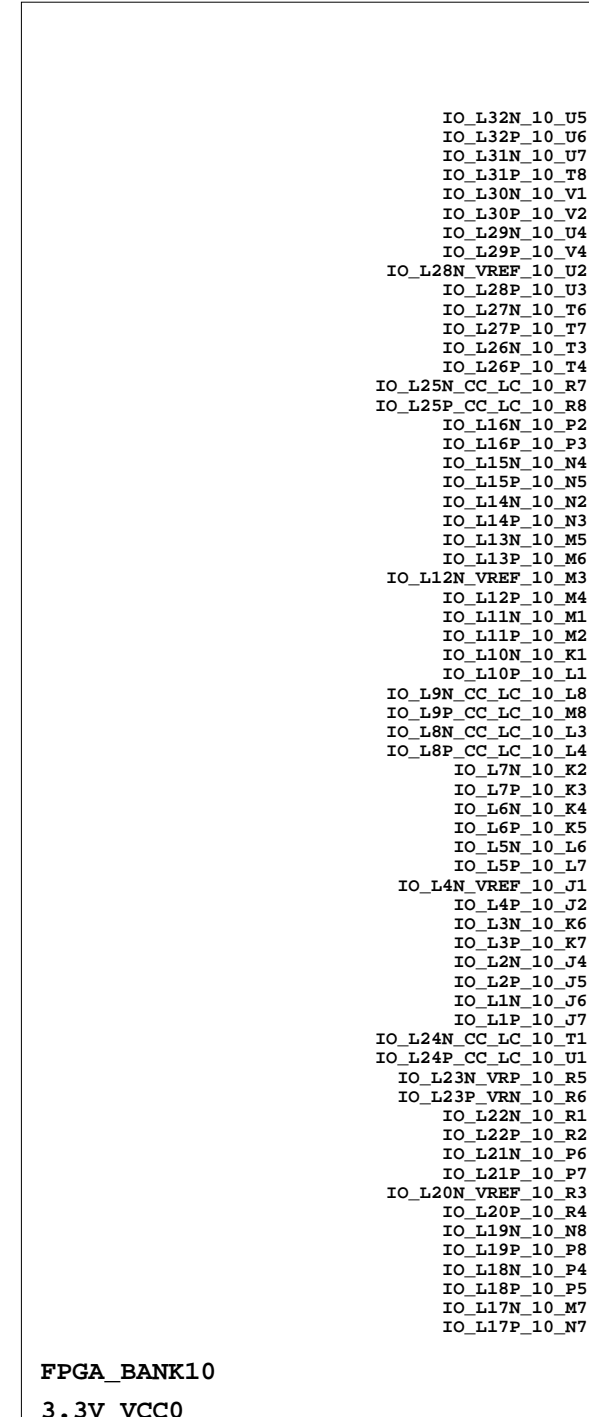
FPGA_BANK8
3.3V VCC0



Title:	
FPGA Bank 7, 8	
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 4 of 24	Drawn By BF



V25	SRAM ZZ		
V26	SRAM MODE		
T19	SRAM FLASH A21		
U20	SRAM FLASH A22		
T20	FLASH A0	2 4.7K	1
T21	FLASH A23	2 4.7K	1
U21	SYSACE MPBRDY		
U22	SYSACE MPA00		
U24	GPIO DIP SW8	2 4.7K	1
U25	GPIO DIP SW7		
V23	GPIO DIP SW6		
U23	GPIO DIP SW5		
U26	GPIO DIP SW4		
T26	GPIO DIP SW3		
R19	GPIO DIP SW2		
R20	GPIO DIP SW1		
N22	FLASH BYTE N		
N23	VGA R0	2 4.7K	1
N24	VGA R1	2 4.7K	1
N25	VGA R2	2 4.7K	1
M22	VGA G0	2 4.7K	1
M23	VGA G1	2 4.7K	1
M20	VGA G2	2 4.7K	1
M21	VGA B0	2 4.7K	1
M26	VGA B1	2 4.7K	1
L26	VGA B2	2 4.7K	1
M24	VGA BLANK N		
M25	VGA PSAVE N		
L23	VGA SYNC N		
L24	BUS ERROR 2		
N19	CPLD IO 1		
M19	CPLD IO 2		
K25	CPLD IO 3		
K26	CPLD IO 4		
K23	CPLD IO 5		
K24	CPLD IO 6		
L20	SRAM DQP0	2 4.7K	1
L21	SRAM DQP1	2 4.7K	1
K20	SRAM DQP2	2 4.7K	1
L19	SRAM DQP3	2 4.7K	1
J25	NC		
J26	NC		
K21	NC		
K22	NC		
J22	NC		
J23	NC		
J20	NC		
J21	NC		
T23	NC		
T24	NC		
R21	NC		
R22	NC		
R23	NC		
R24	NC		
P19	NC		
P20	NC		
R25	NC		
R26	NC		
P22	NC		
P23	NC		
P24	NC		
P25	NC		
N20	NC		
N21	NC		

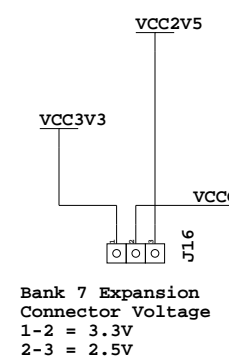
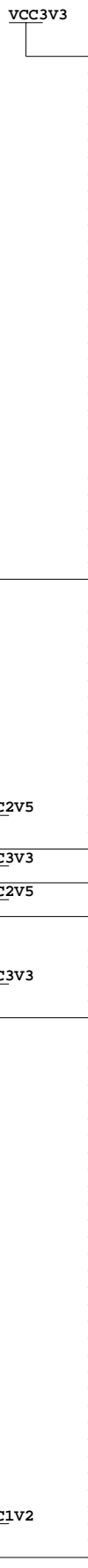
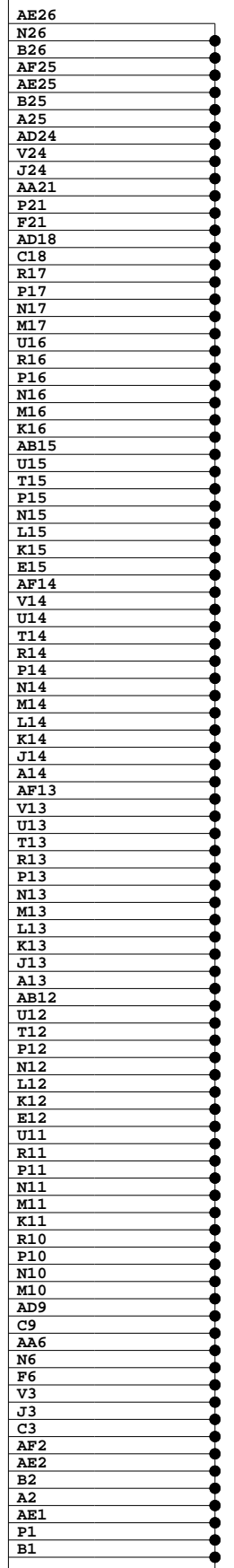


U5	NC		
U6	NC		
U7	NC		
T8	NC		
T8	NC		
V1	NC		
V2	NC		
U4	NC		
V4	NC		
U2	NC		
U3	NC		
T6	NC		
T7	NC		
T7	NC		
T3	NC		
T4	NC		
R7	NC		
R8	NC		
P2	NC		
P2	NC		
P3	NC		
N4	NC		
N5	NC		
N2	NC		
N3	NC		
M5	NC		
M6	NC		
M3	NC		
M4	NC		
M1	NC		
M2	NC		
K1	NC		
L1	NC		
L8	NC		
M8	NC		
L3	NC		
L4	NC		
K2	NC		
K3	NC		
K4	NC		
K5	NC		
L6	NC		
L7	NC		
J1	NC		
J2	NC		
K6	NC		
K7	NC		
J4	NC		
J5	NC		
J6	NC		
J7	NC		
T1	NC		
U1	NC		
R5	NC		
R6	NC		
R1	NC		
R2	NC		
P6	NC		
P7	NC		
R3	NC		
R4	NC		
N8	NC		
P8	NC		
P4	NC		
P5	NC		
M7	NC		
N7	NC		



Title:	
FPGA Bank 9, 10	
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 5 of 24	Drawn By BF

GND_AE26
GND_N26
GND_B26
GND_AF25
GND_AE25
GND_B25
GND_A25
GND_AD24
GND_V24
GND_J24
GND_AA21
GND_F21
GND_P21
GND_AD18
GND_C18
GND_R17
GND_P17
GND_N17
GND_M17
GND_U16
GND_R16
GND_P16
GND_N16
GND_M16
GND_K16
GND_AB15
GND_U15
GND_T15
GND_P15
GND_N15
GND_L15
GND_K15
GND_E15
GND_AF14
GND_V14
GND_U14
GND_T14
GND_R14
GND_P14
GND_N14
GND_M14
GND_L14
GND_K14
GND_J14
GND_A14
GND_AF13
GND_V13
GND_U13
GND_T13
GND_R13
GND_P13
GND_N13
GND_M13
GND_L13
GND_K13
GND_J13
GND_A13
GND_AB12
GND_U12
GND_T12
GND_P12
GND_N12
GND_L12
GND_K12
GND_E12
GND_U11
GND_R11
GND_P11
GND_N11
GND_M11
GND_K11
GND_R10
GND_P10
GND_N10
GND_M10
GND_AD9
GND_C9
GND_AA6
GND_N6
GND_F6
GND_V3
GND_J3
GND_C3
GND_AF2
GND_AE2
GND_B2
GND_A2
GND_AE1
GND_P1
GND_B1

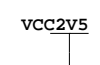


R9 VCCO_10_R9
U8 VCCO_10_U8
K8 VCCO_10_K8
T5 VCCO_10_T5
L5 VCCO_10_L5
T2 VCCO_10_T2
L2 VCCO_10_L2
N1 VCCO_10_N1
P26 VCCO_9_P26
T25 VCCO_9_T25
L25 VCCO_9_L25
T22 VCCO_9_T22
L22 VCCO_9_L22
U19 VCCO_9_U19
K19 VCCO_9_K19
M18 VCCO_9_M18
W9 VCCO_8_W9
AE8 VCCO_8_AE8
AB8 VCCO_8_AB8
W8 VCCO_8_W8
V8 VCCO_8_V8
AE5 VCCO_8_AE5
AA5 VCCO_8_AA5
AA2 VCCO_8_AA2
AA25 VCCO_7_AA25
AE22 VCCO_7_AE22
AA22 VCCO_7_AA22
AE19 VCCO_7_AE19
AB19 VCCO_7_AB19
V19 VCCO_7_V19
W18 VCCO_7_W18
W17 VCCO_7_W17
H10 VCCO_6_H10
H9 VCCO_6_H9
J8 VCCO_6_J8
E8 VCCO_6_E8
B8 VCCO_6_B8
F5 VCCO_6_F5
B5 VCCO_6_B5
F2 VCCO_6_F2
F25 VCCO_5_F25
F22 VCCO_5_F22
B22 VCCO_5_B22
J19 VCCO_5_J19
H19 VCCO_5_H19
E19 VCCO_5_E19
B19 VCCO_5_B19
H18 VCCO_5_H18
AD15 VCCO_4_AD15
AE11 VCCO_4_AE11
B16 VCCO_3_B16
B11 VCCO_3_B11
AB16 VCCO_2_AB16
E16 VCCO_2_E16
E11 VCCO_1_E11
J15 VCCO_0_J15
V12 VCCO_0_V12
U18 VCCINT_U18
T18 VCCINT_T18
L18 VCCINT_L18
K18 VCCINT_K18
V17 VCCINT_V17
U17 VCCINT_U17
T17 VCCINT_T17
L17 VCCINT_L17
K17 VCCINT_K17
J17 VCCINT_J17
V16 VCCINT_V16
T16 VCCINT_T16
L16 VCCINT_L16
J16 VCCINT_J16
R15 VCCINT_R15
M15 VCCINT_M15
R12 VCCINT_R12
M12 VCCINT_M12
V11 VCCINT_V11
T11 VCCINT_T11
L11 VCCINT_L11
J11 VCCINT_J11
V10 VCCINT_V10
U10 VCCINT_U10
T10 VCCINT_T10
L10 VCCINT_L10
K10 VCCINT_K10
J10 VCCINT_J10
U9 VCCINT_U9
T9 VCCINT_T9
L9 VCCINT_L9
K9 VCCINT_K9

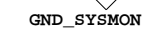
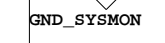
FPGA_PWR

VCCAUX_R18
VCCAUX_P18
VCCAUX_N18
VCCAUX_H17
VCCAUX_W16
VCCAUX_H16
VCCAUX_V15
VCCAUX_J12
VCCAUX_W11
VCCAUX_H11
VCCAUX_W10
VCCAUX_P9
VCCAUX_N9
VCCAUX_M9
AVSS_SM_AE17
AVDD_SM_AF17
VREFP_SM_AE16
VREFN_SM_AE15

R18
P18
N18
H17
W16
H16
V15
J12
W11
H11
W10
P9
N9
M9
AE17
AF17
AE16
AE15



SYS_MON_VREFN_AVSS
SYS_MON_AVDD
SYS_MON_VREFP
SYS_MON_VREFN_AVSS

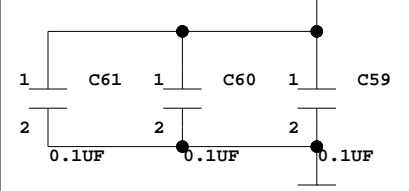
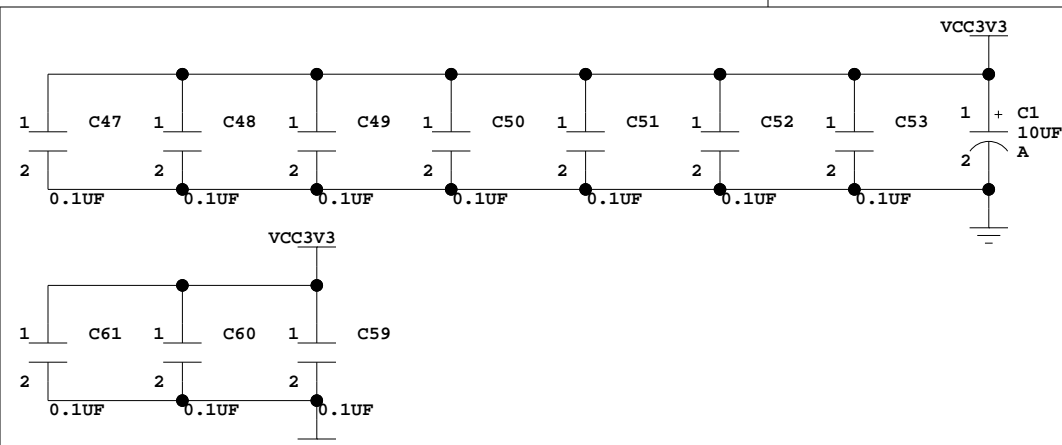


FPGA_GND



Title: FPGA Ground and Power	
Date:	Ver:
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U1

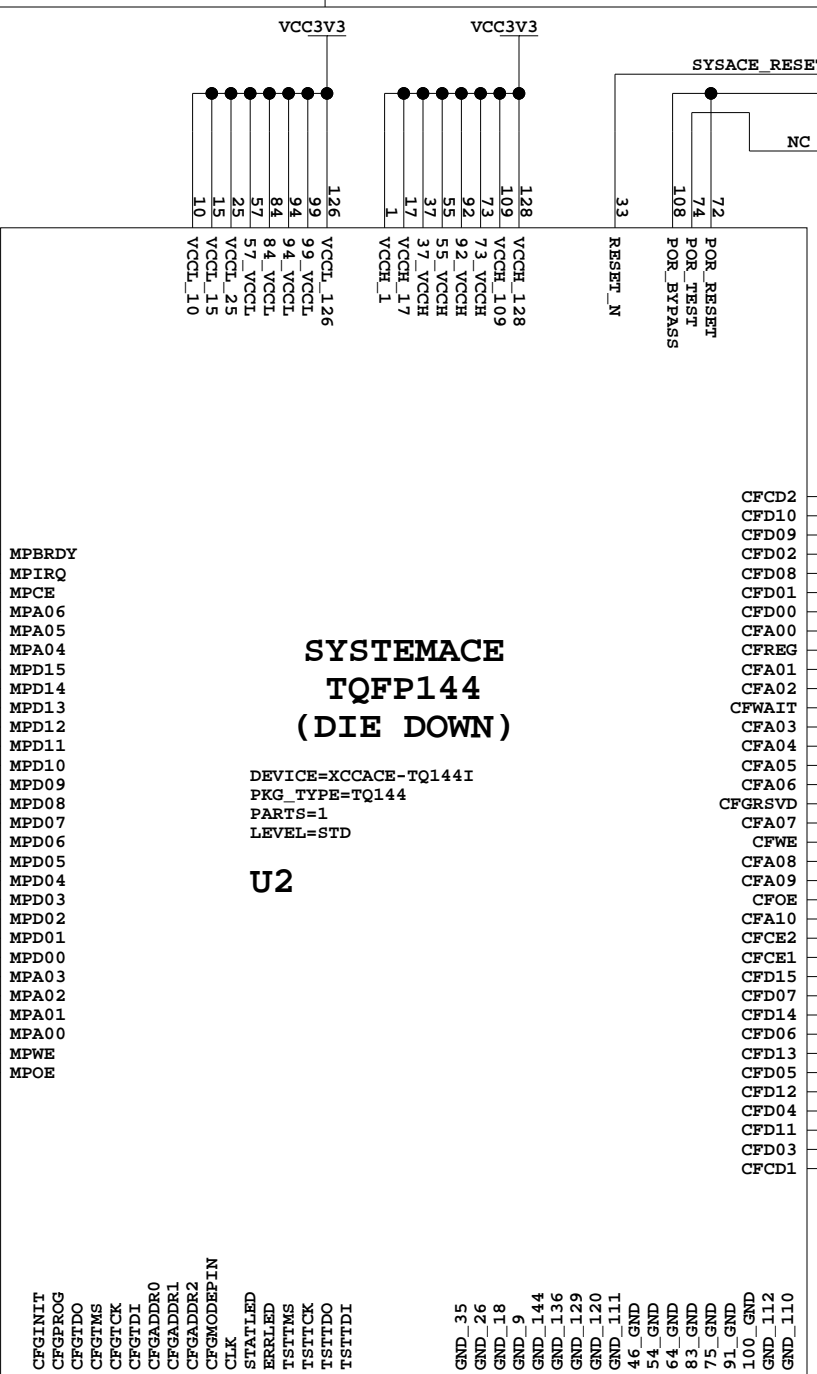


■	SYSACE MPBRDY	39	MPBRDY
■	SYSACE MPIRQ	41	MPIRQ
■	SYSACE MPCE	42	MPCE
■	SYSACE MPA06	43	MPA06
■	SYSACE MPA05	44	MPA05
■	SYSACE MPA04	45	MPA04
■	SYSACE USB D15	47	MPD15
■	SYSACE USB D14	48	MPD14
■	SYSACE USB D13	49	MPD13
■	SYSACE USB D12	50	MPD12
■	SYSACE USB D11	51	MPD11
■	SYSACE USB D10	52	MPD10
■	SYSACE USB D9	53	MPD09
■	SYSACE USB D8	56	MPD08
■	SYSACE USB D7	58	MPD07
■	SYSACE USB D6	59	MPD06
■	SYSACE USB D5	60	MPD05
■	SYSACE USB D4	61	MPD04
■	SYSACE USB D3	62	MPD03
■	SYSACE USB D2	63	MPD02
■	SYSACE USB D1	65	MPD01
■	SYSACE USB D0	66	MPD00
■	SYSACE MPA03	67	MPA03
■	SYSACE A2 USB A1	68	MPA02
■	SYSACE A1 USB A0	69	MPA01
■	SYSACE MPA00	70	MPA00
■	SYSACE MPWE USB WR_N	76	MPWE
■	SYSACE MPOE USB RD_N	77	MPOE

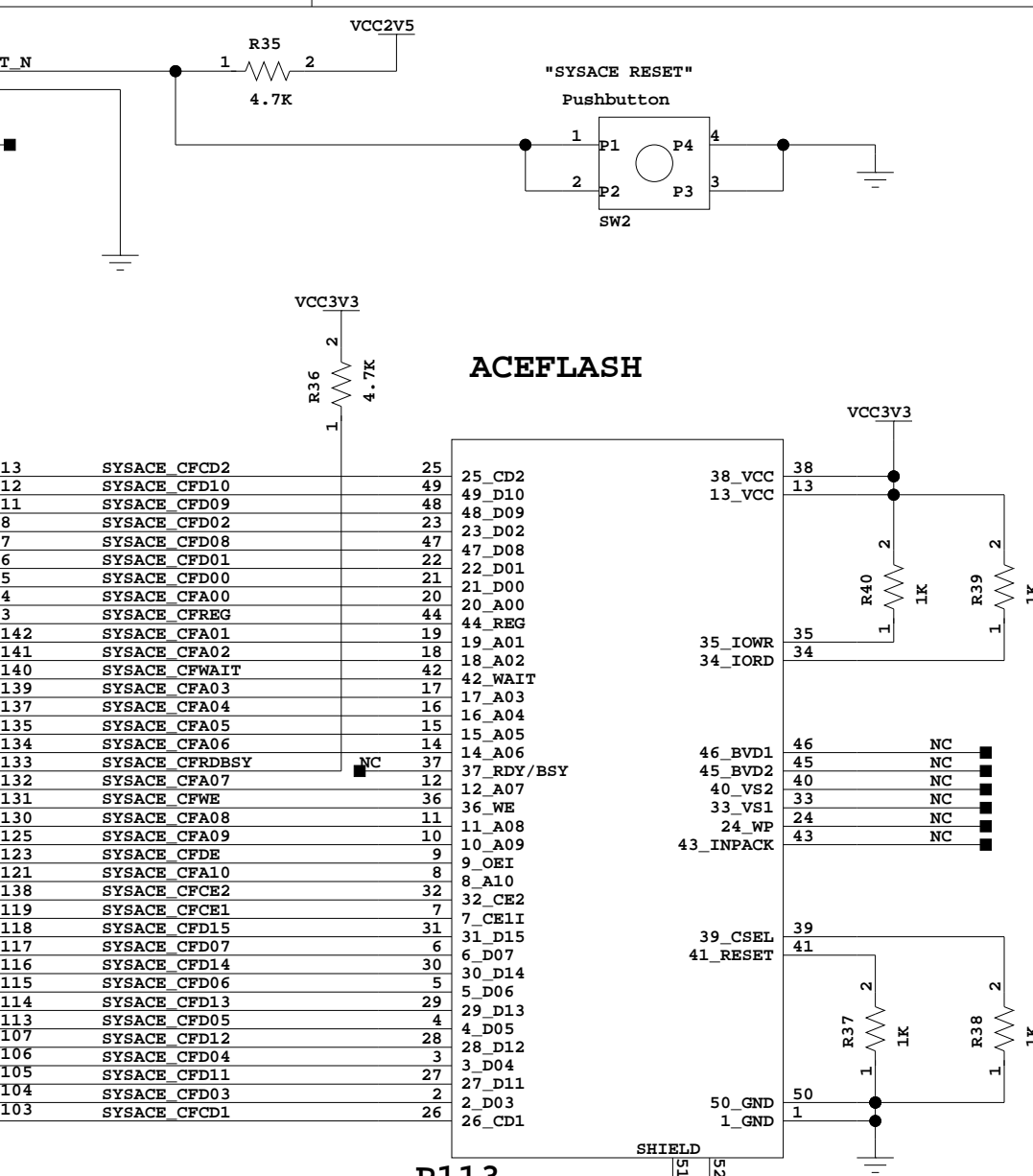
**SYSTEMACE
TQFP144
(DIE DOWN)**

DEVICE=XCCACE-TQ144I
PKG_TYPE=TQ144
PARTS=1
LEVEL=STD

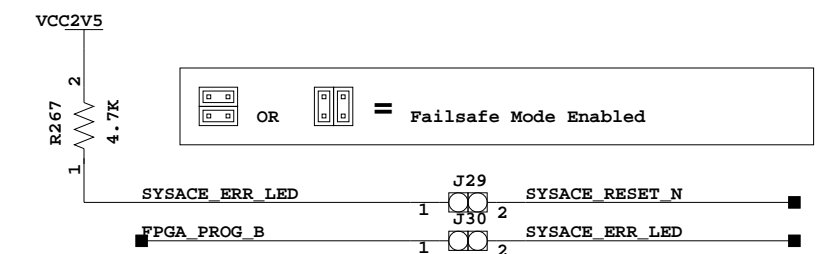
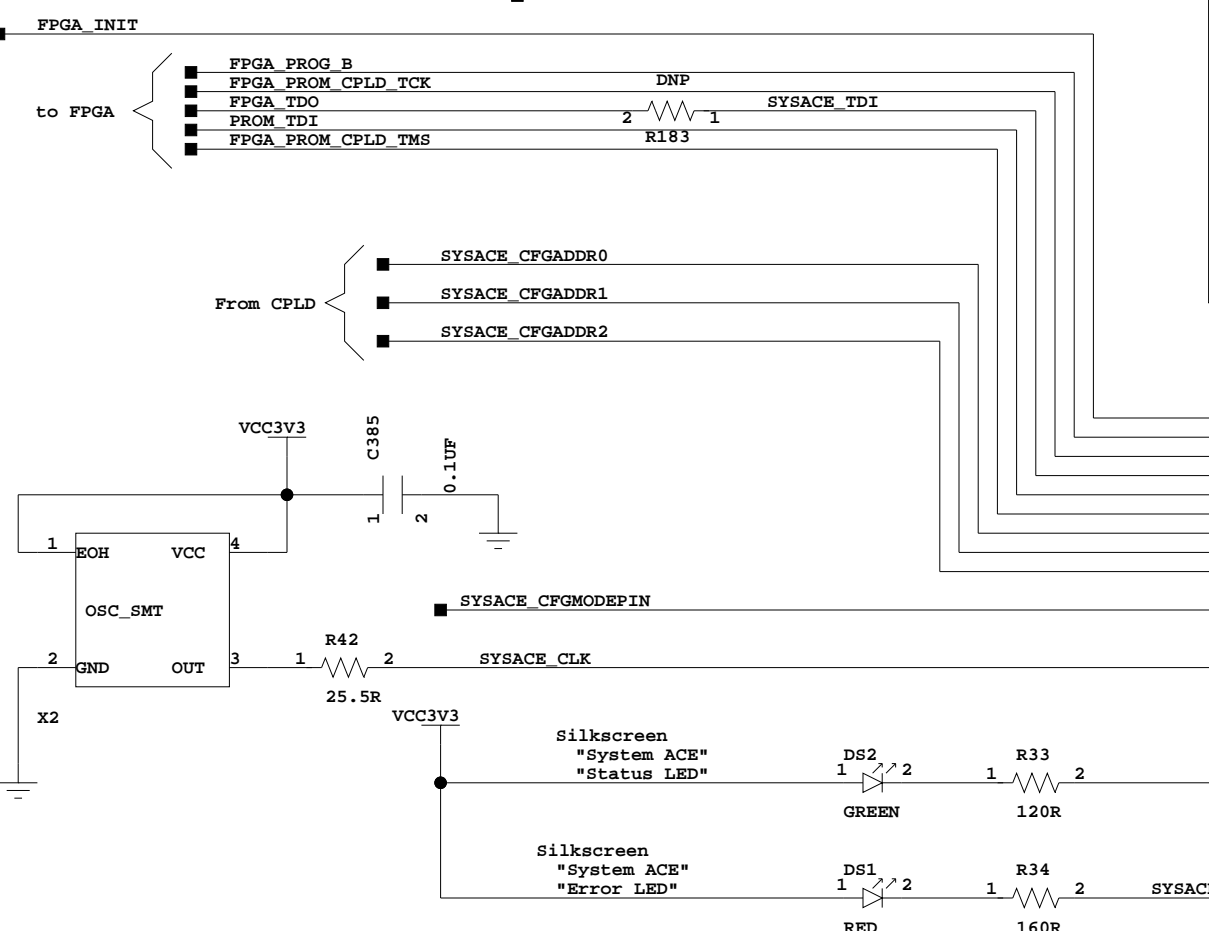
U2



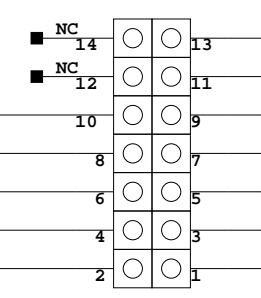
ACEFLASH



P113



Combined
FPGA & CPU
PC4 Connector
J20



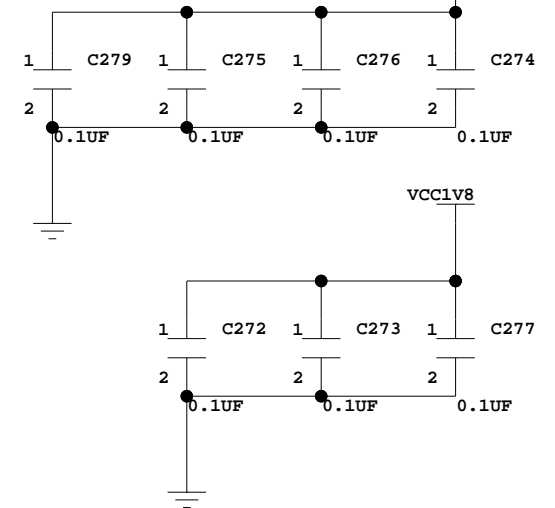
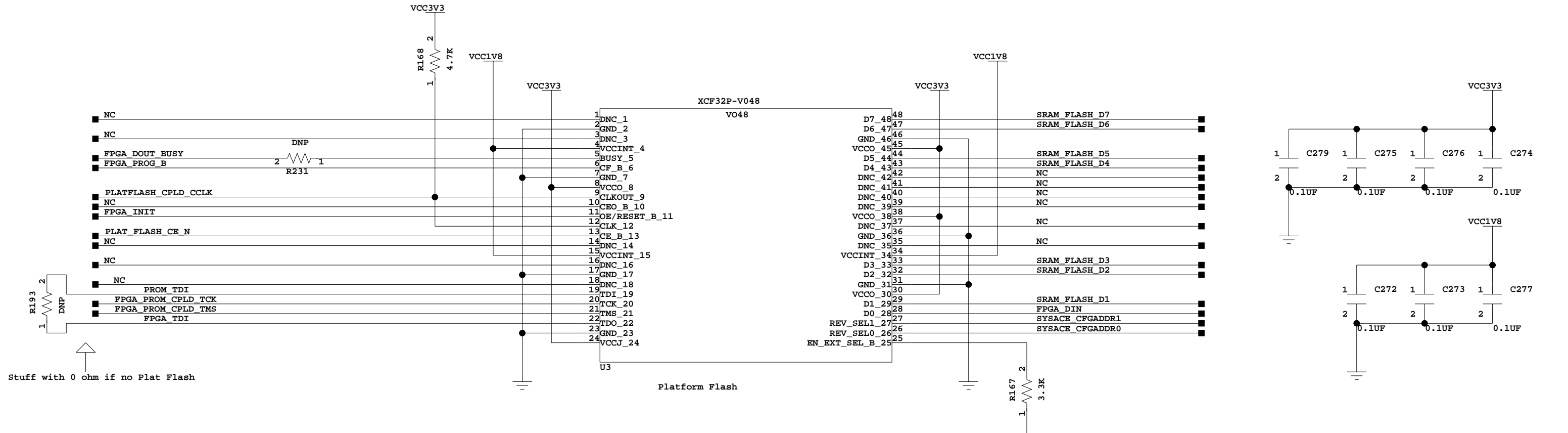
XILINX

Title: System ACE

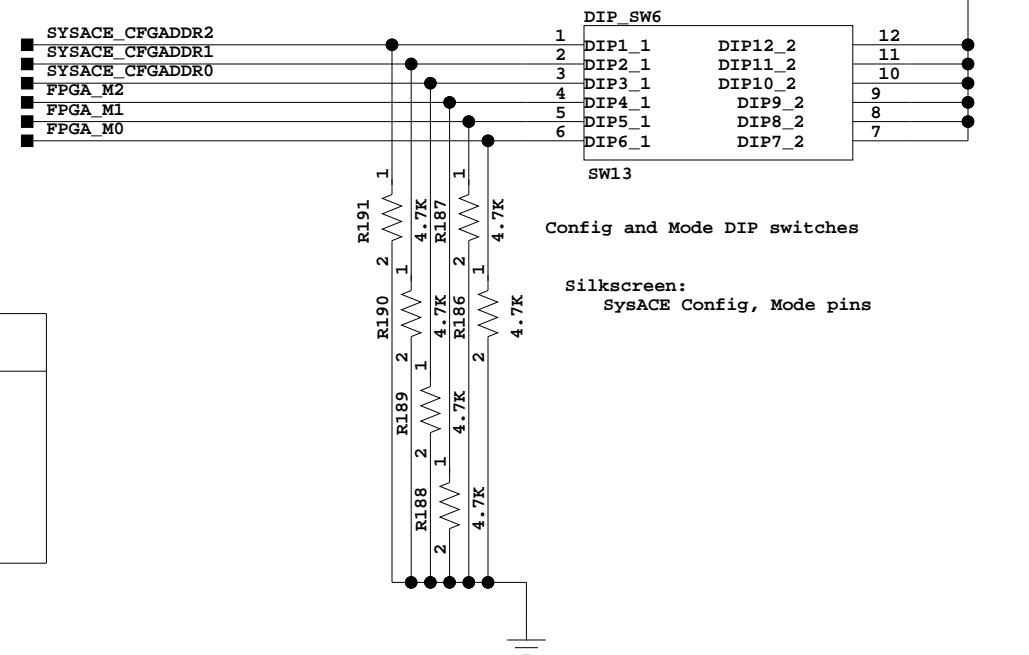
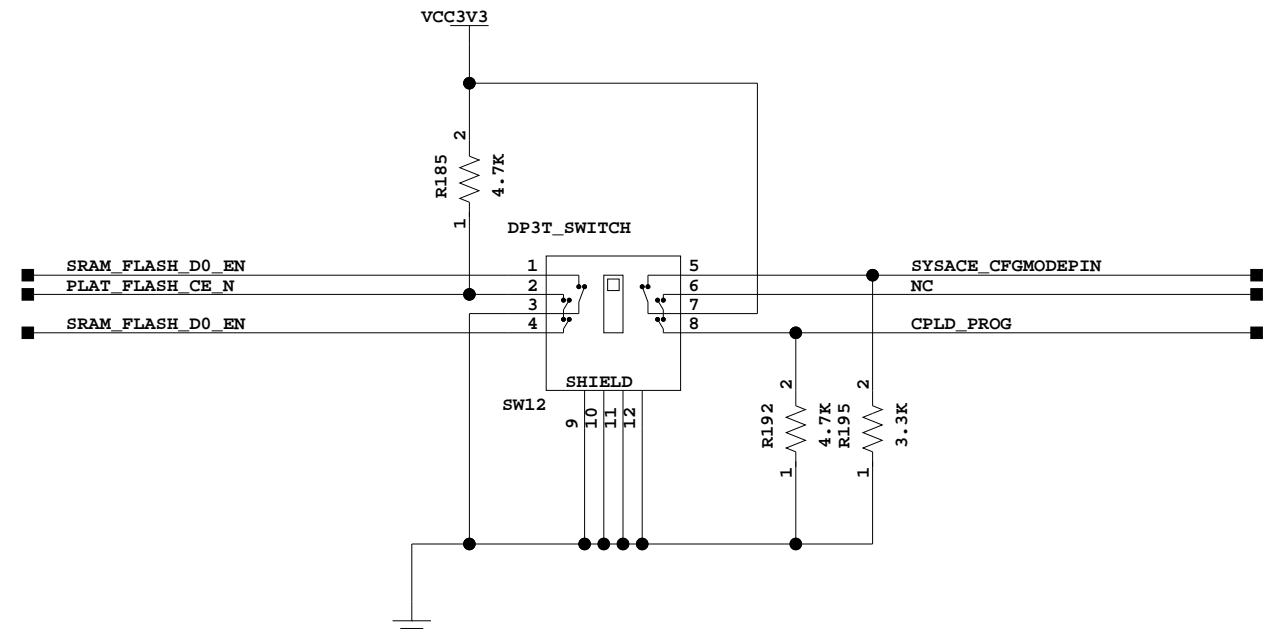
Date: _____ Ver: _____

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Sheet 7 of 24 Drawn By BF

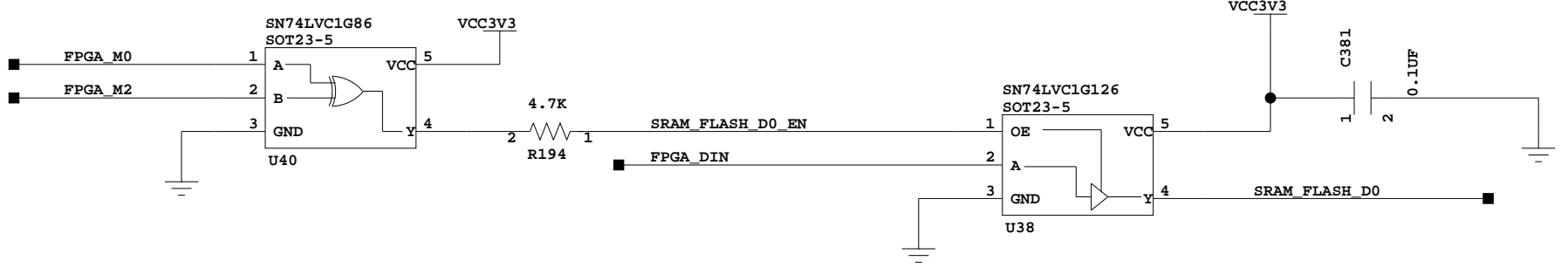


System ACE / Platform Flash / CPLD Flash Configuration Switch



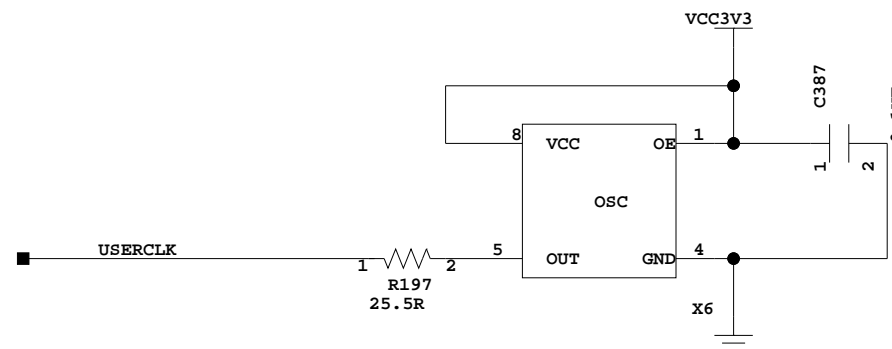
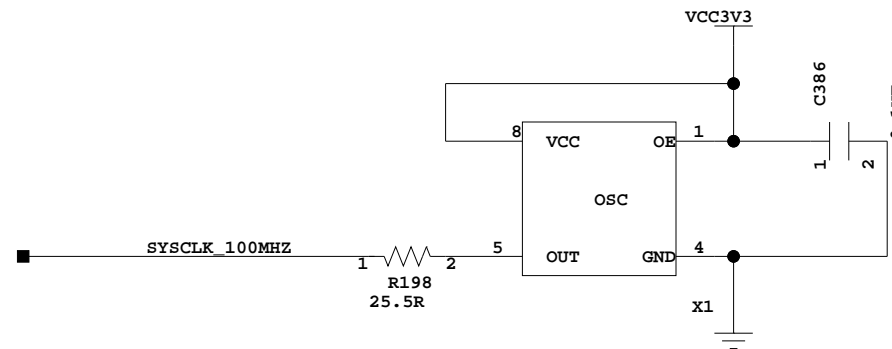
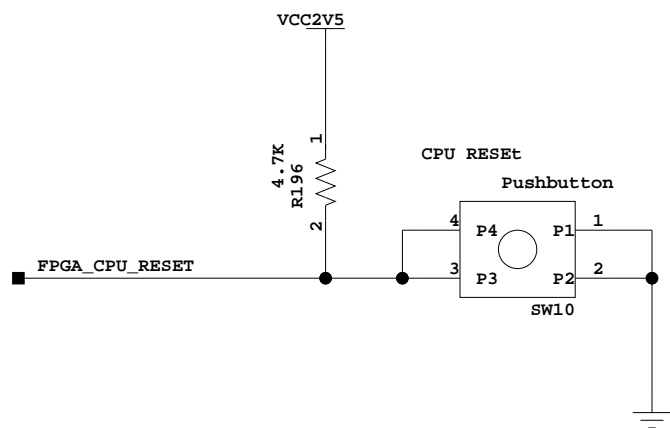
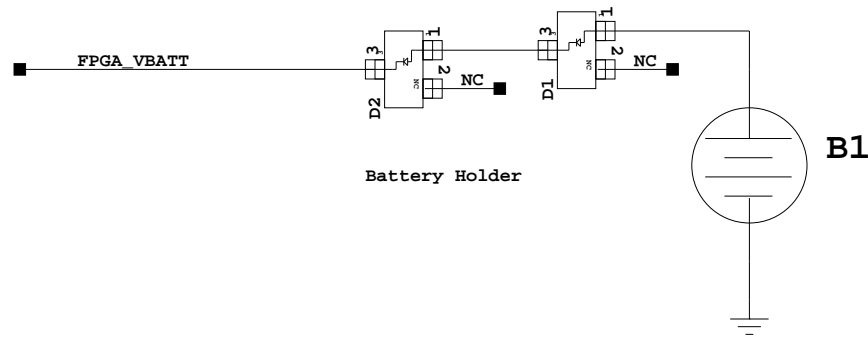
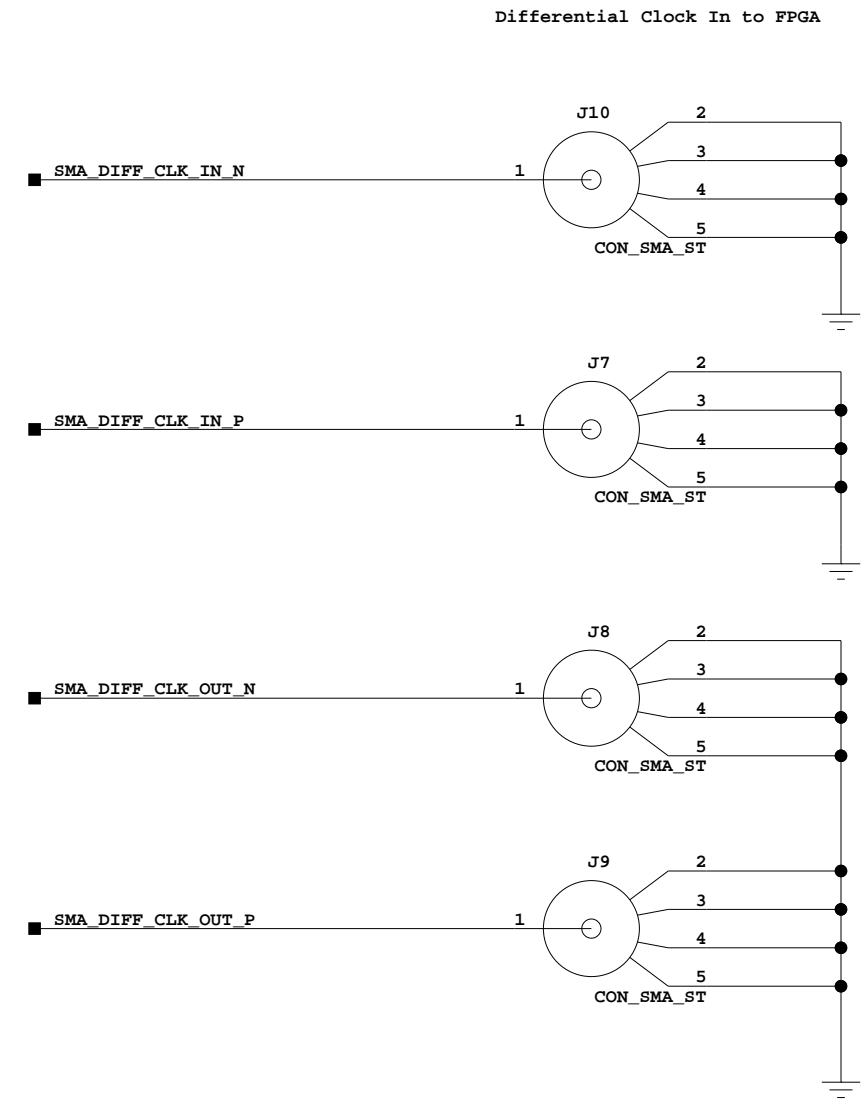
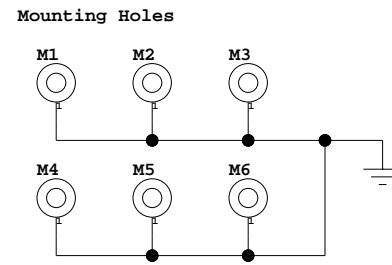
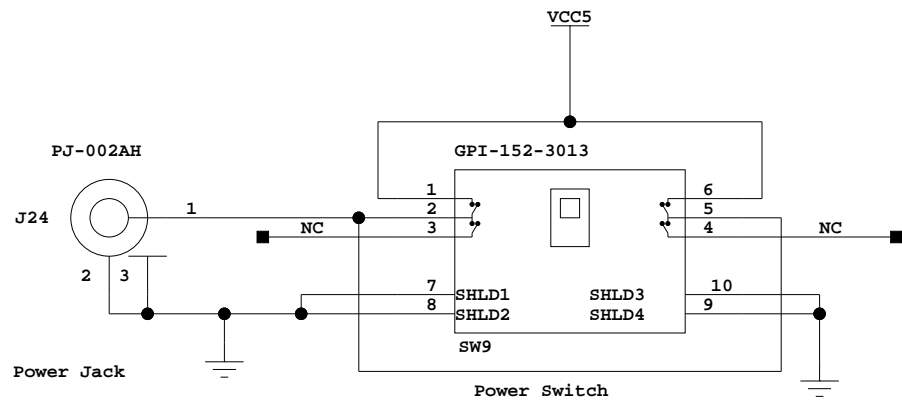
m0	m2	Cfg Switch	D0/DIN Short
0	0	SysACE/CPLD	OPEN
0	1	SysACE/CPLD	OPEN
1	0	SysACE/CPLD	OPEN
1	1	SysACE/CPLD	OPEN
0	0	Plat FLASH	OPEN
0	1	Plat FLASH	SHORT
1	0	Plat FLASH	SHORT
1	1	Plat FLASH	OPEN

Toggles connection from Plat Flash D0 to SRAM D0



Title: Platform Flash

Date:	Ver:
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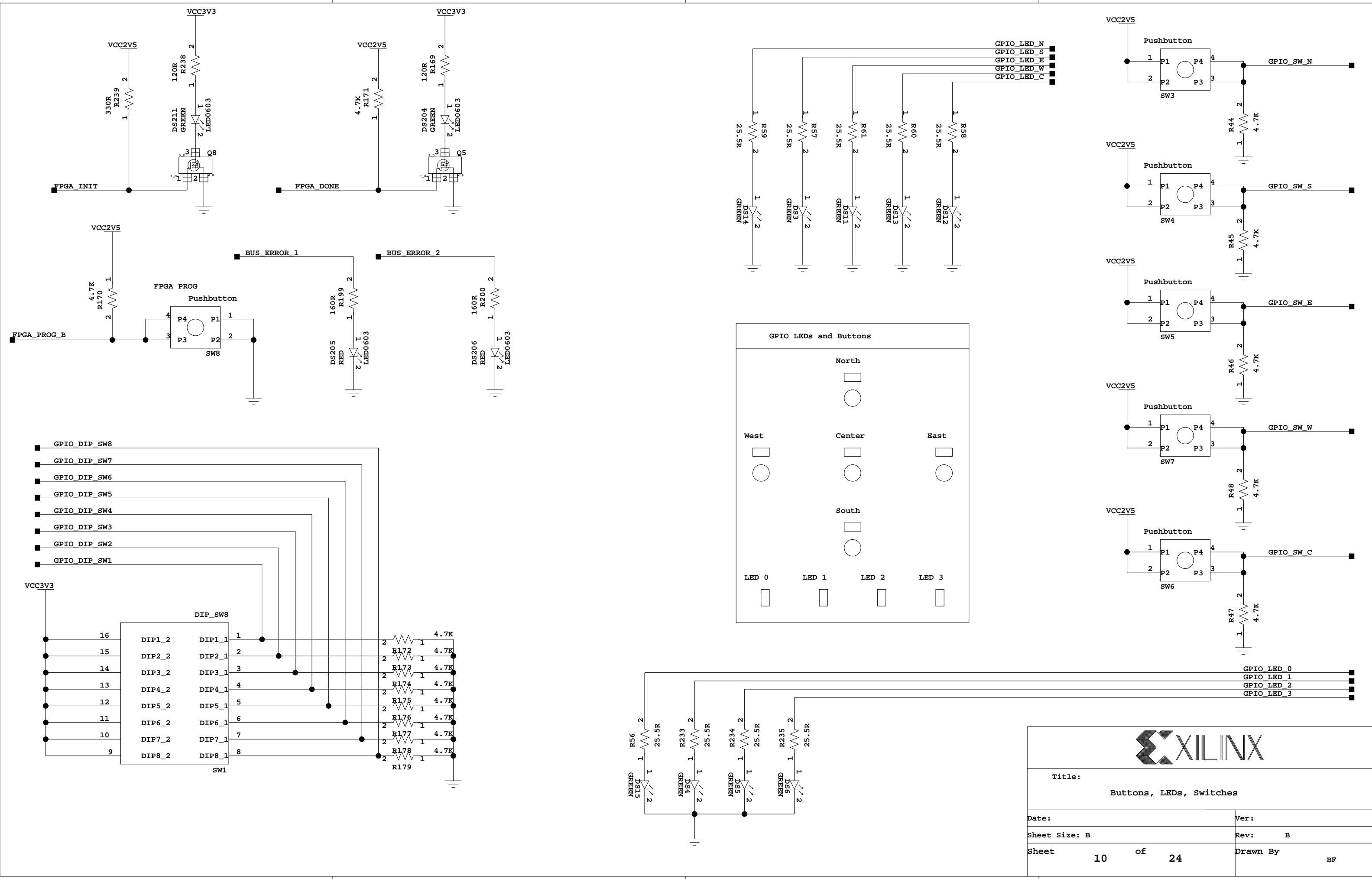


Differential Clock Out from FPGA

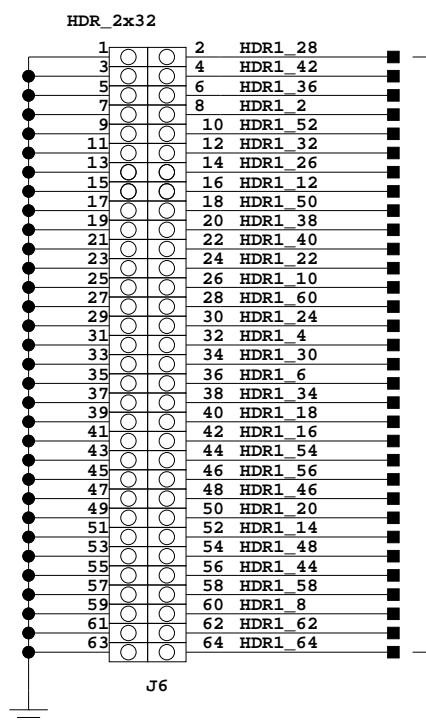
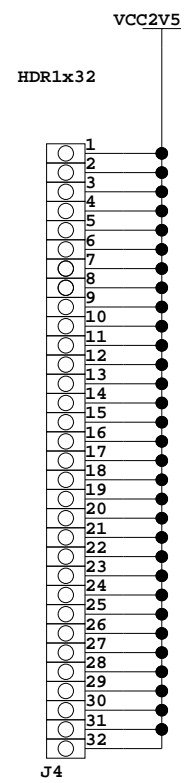


Title:
SMA Connectors, Power Switch,
Battery, Oscillators, Reset

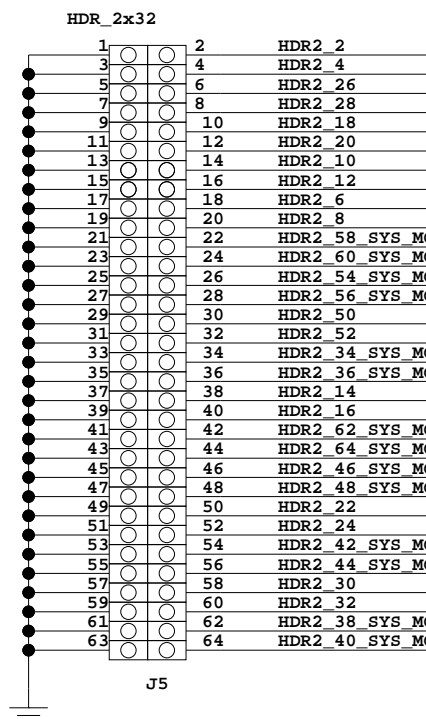
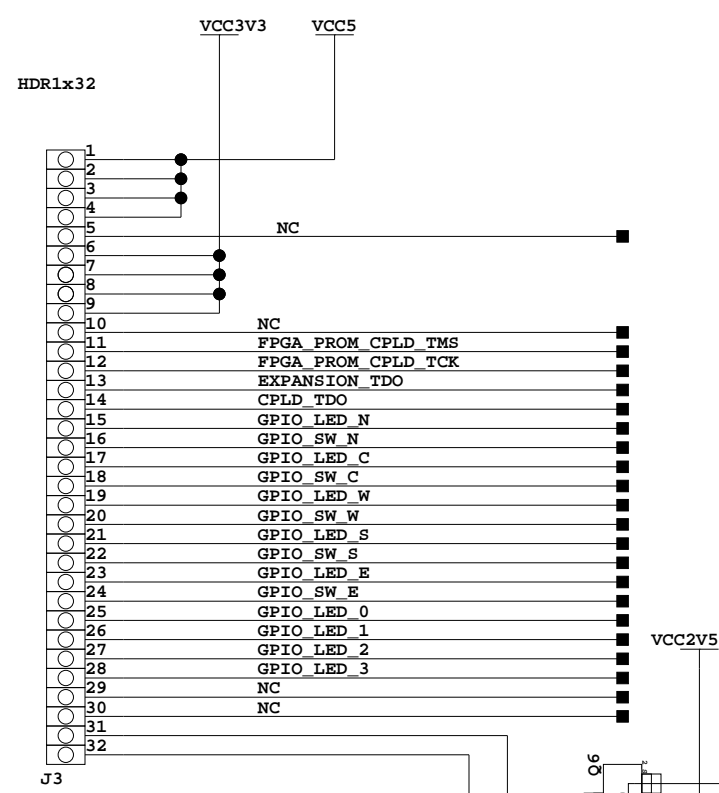
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 9 of 24	Drawn By BF



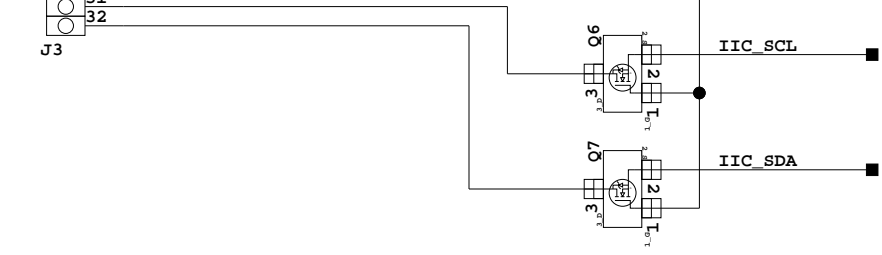
Title: Buttons, LEDs, Switches	
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 10 of 24	Drawn By BF



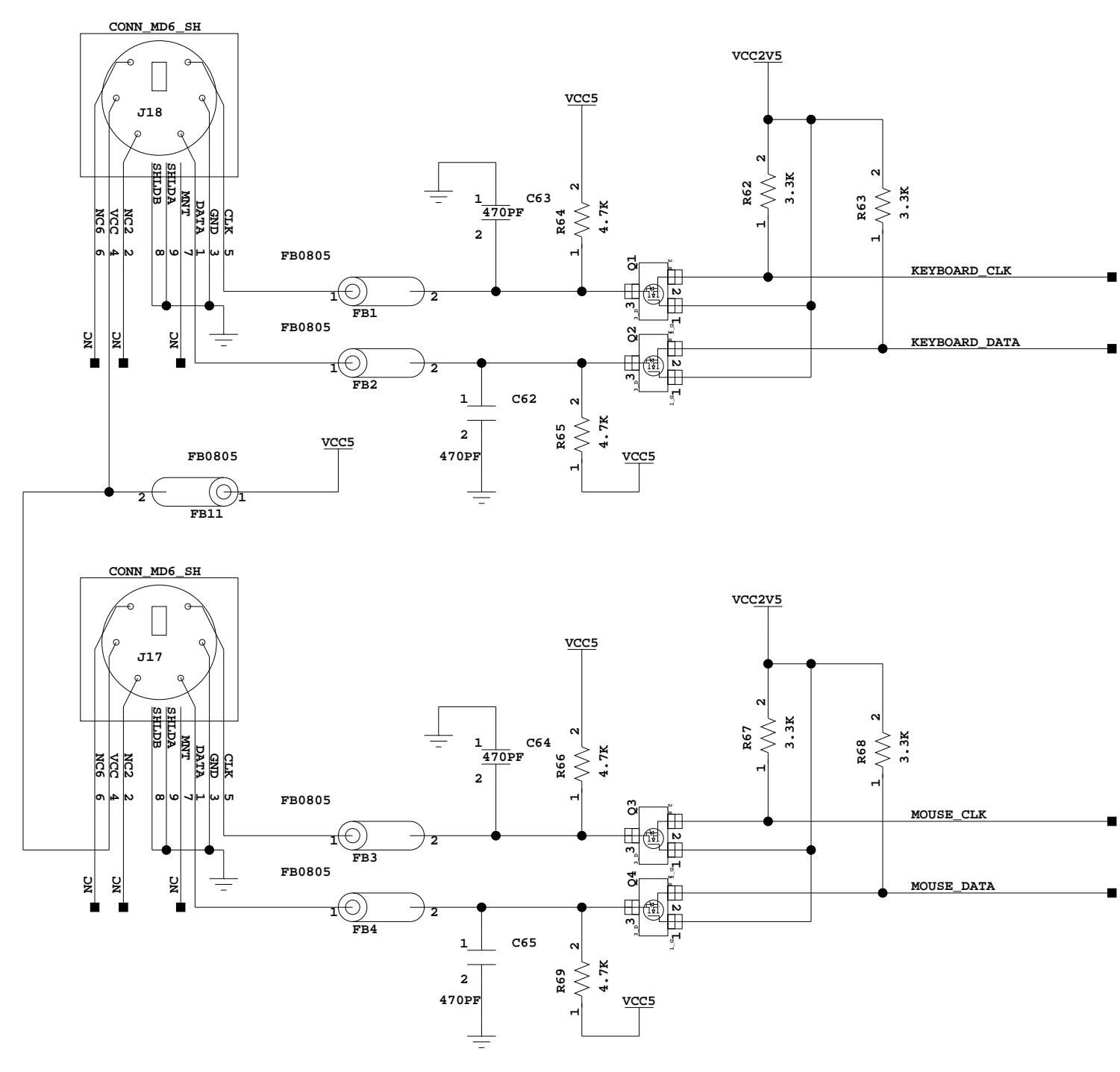
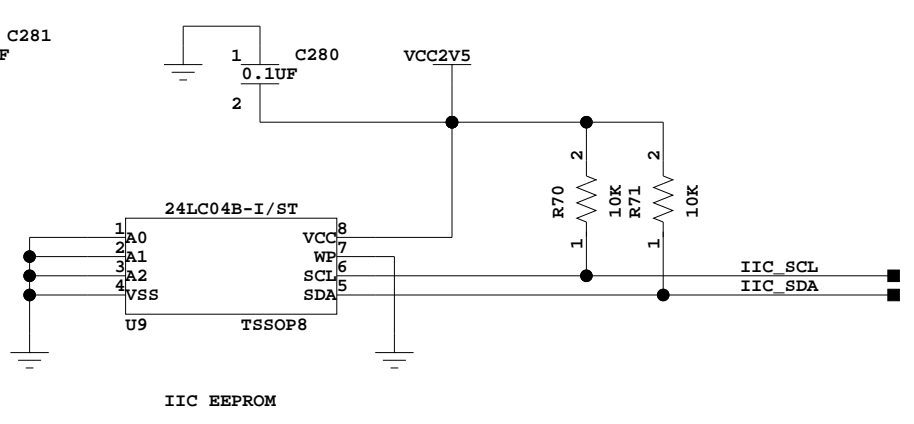
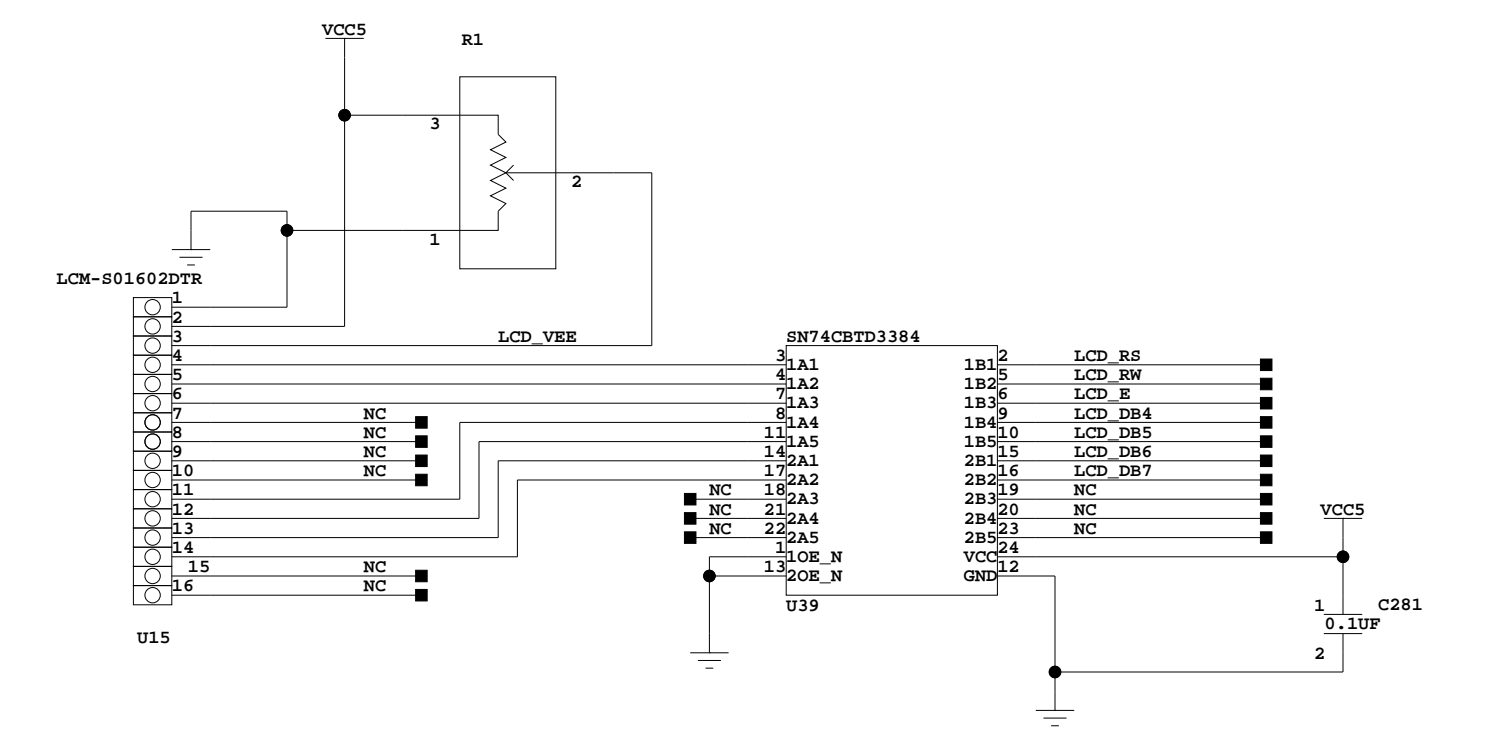
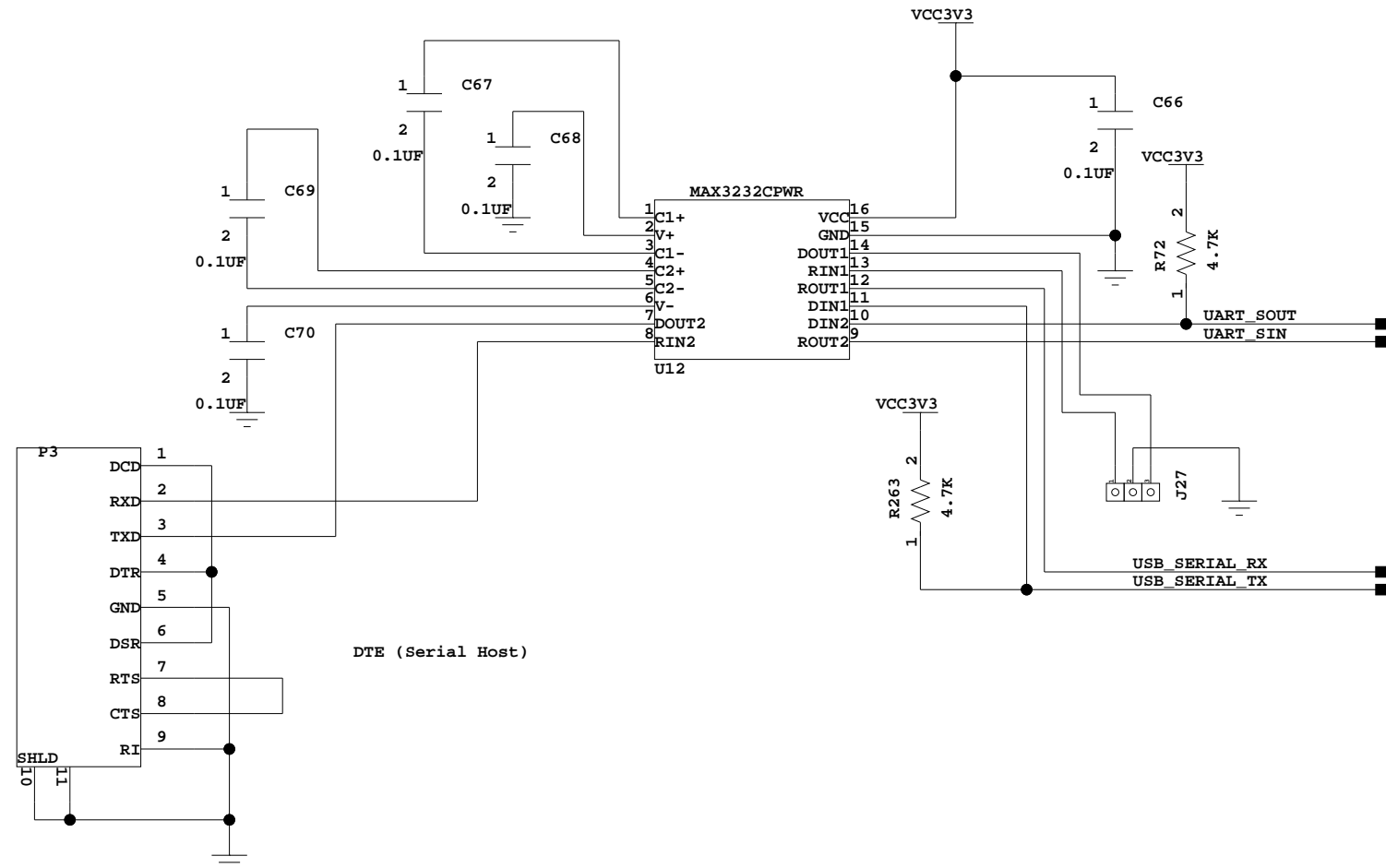
Matched Length Traces
Independent signals



Matched Length Traces
Differential Pairs

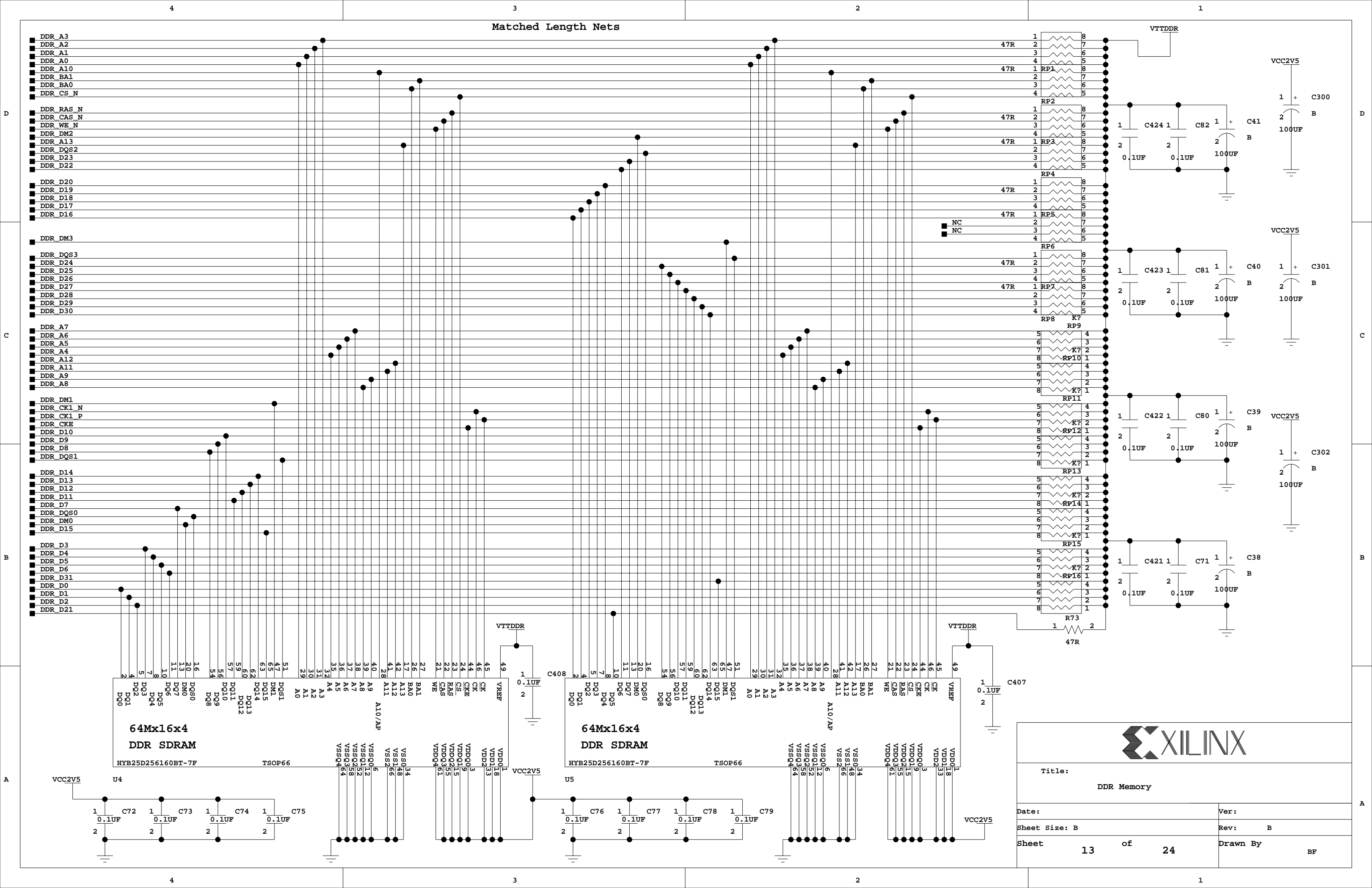


Title:	
Expansion Headers	
Date:	Ver:
Sheet Size: B	Rev: B
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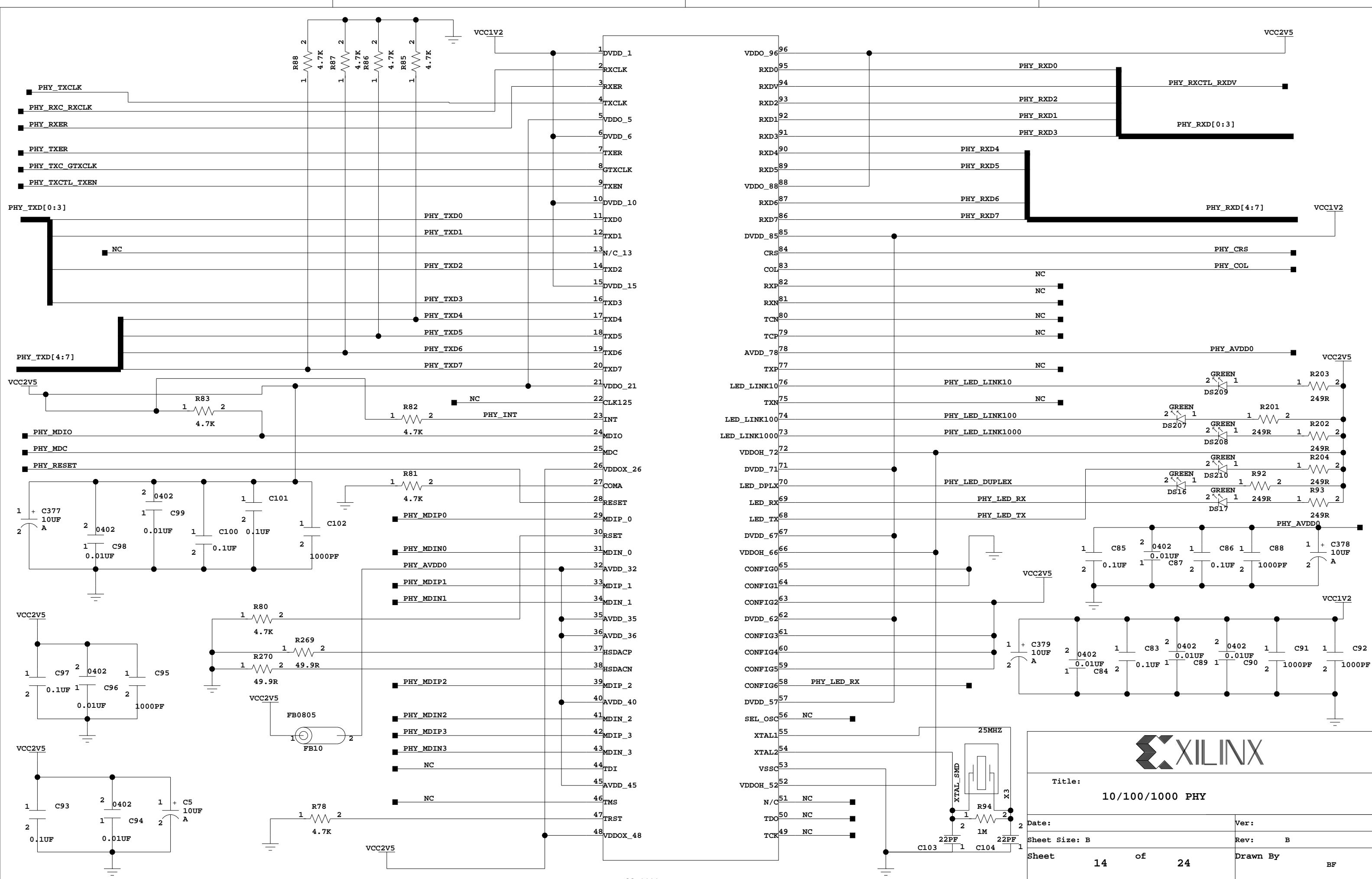


Title: LCD, PS2, UART, IIC EEPROM	
Date:	Ver:
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Sheet 12 of 24	Drawn By BF

Matched Length Nets



Title: DDR Memory	
Date:	Ver:
Sheet Size: B	Rev: B
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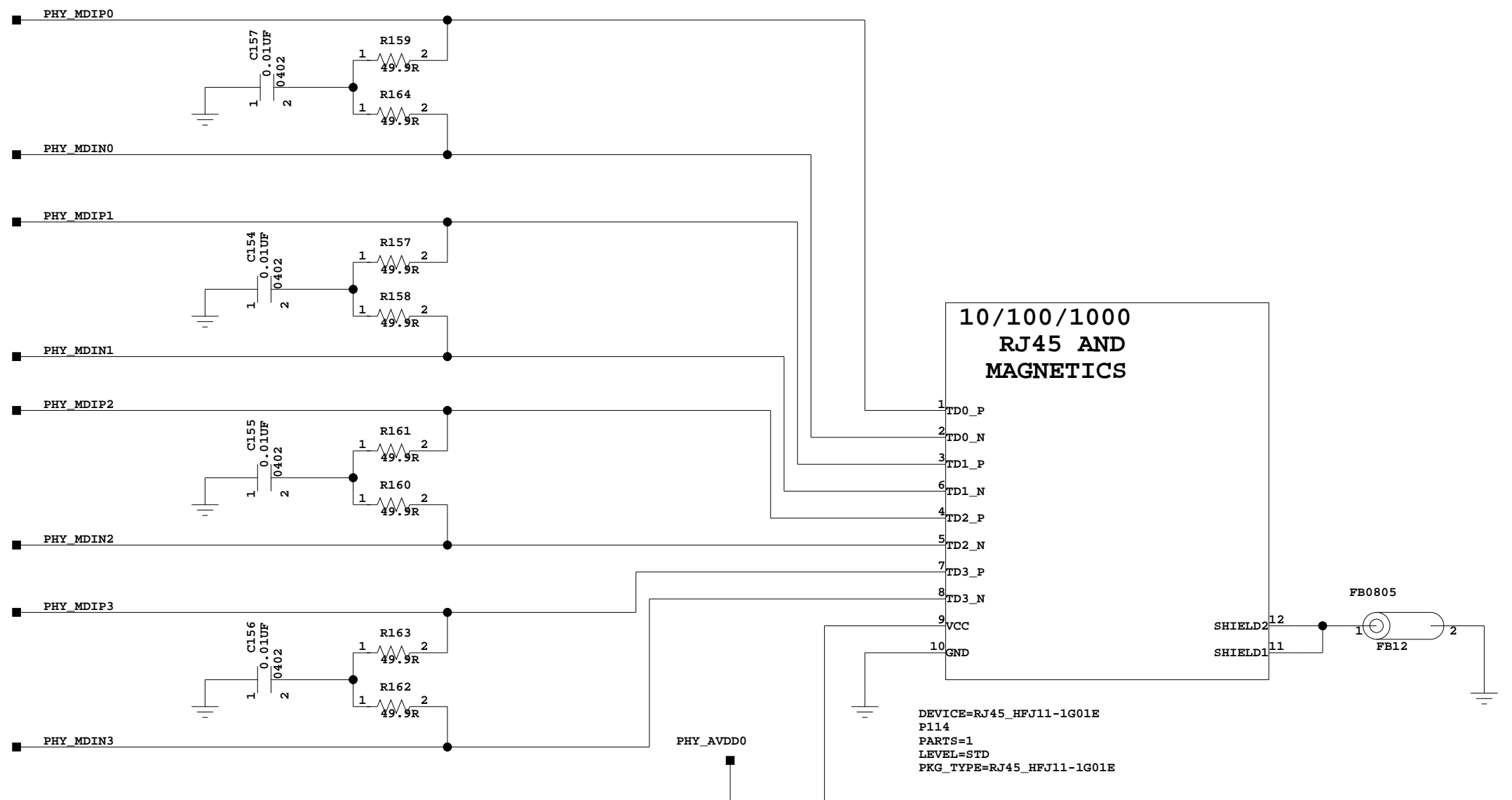
DEVICE=M88E1111
U45
PARTS=1

XILINX

Title: 10/100/1000 PHY

Date:	Ver:
Sheet Size: B	Rev: B
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Pin to Constant Mapping	
Pin	Bit[2:0]
VCC2V5	111
PHY_LED_LINK10	110
PHY_LED_LINK100	101
PHY_LED_LINK1000	100
PHY_LED_DUPLEX	011
PHY_LED_RX	010
PHY_LED_TX	001
GND	000

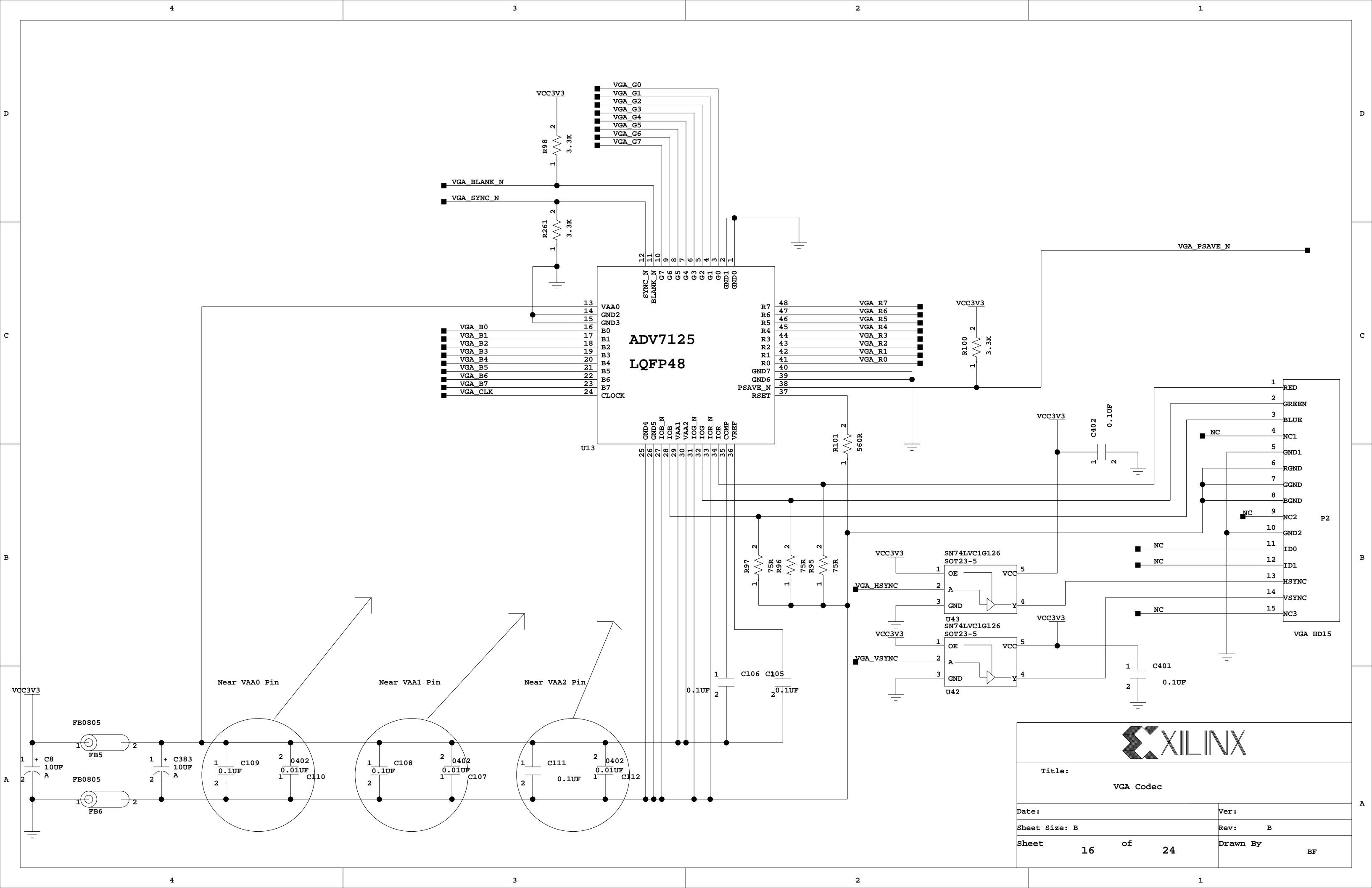


Pin	Bit[2]	Bit[1]	Bit[0]		
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000	PHYAddress "00000". Do not advertise the PAUSE bit
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg enabled, advertise all capabilities; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CONFIG3	ANEG[0]	ENA_XC	DIS_125	111	
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]	111	GMII to Cu mode. Fiber/copper auto-detect disabled. Sleep mode disabled.
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]	111	
CONFIG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active LOW Interrupt. 50ohm SERDES option.

XILINX

Title:
RJ45 Connector and PHY Decoupling

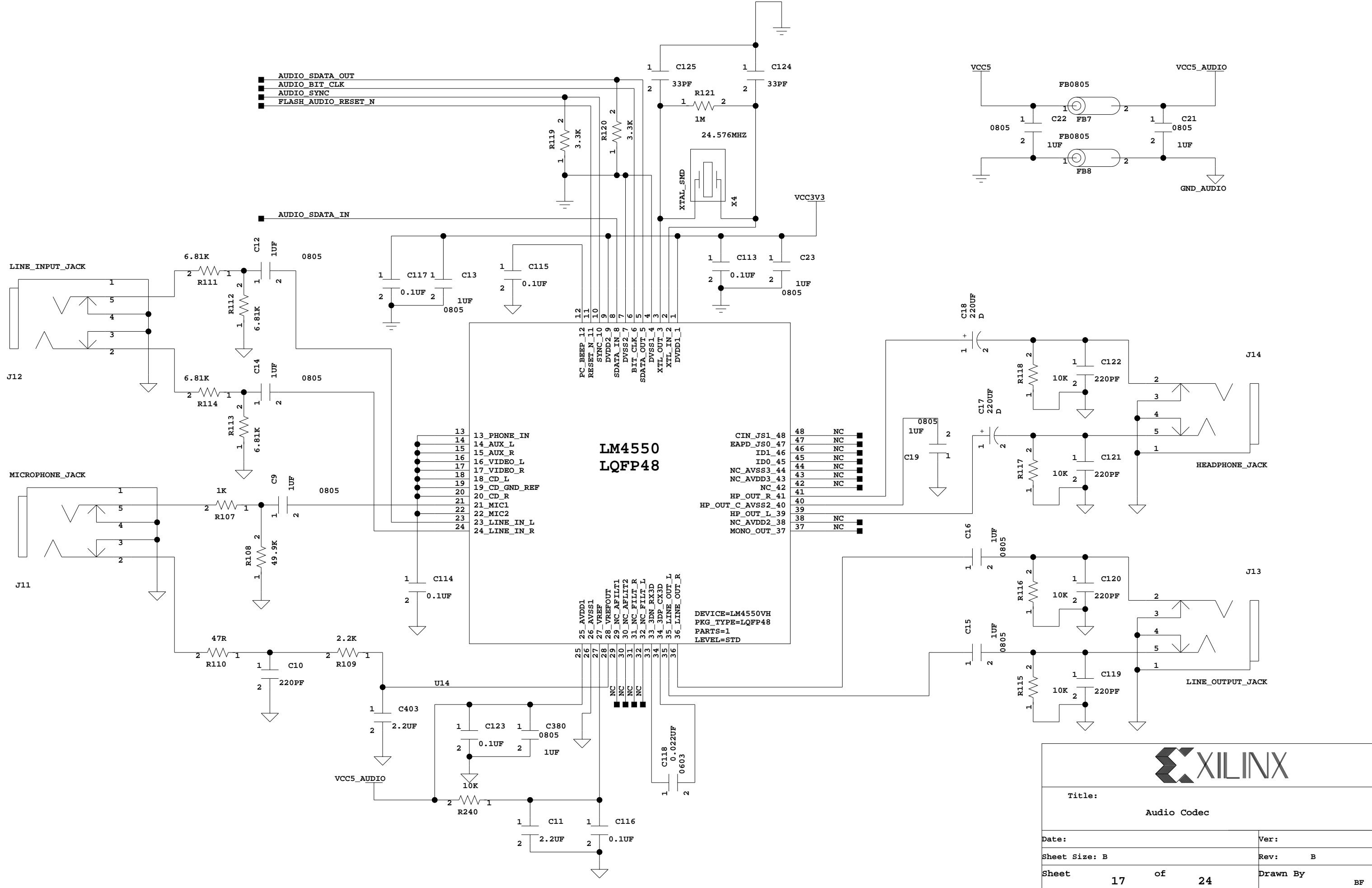
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 15 of 24	Drawn By BF



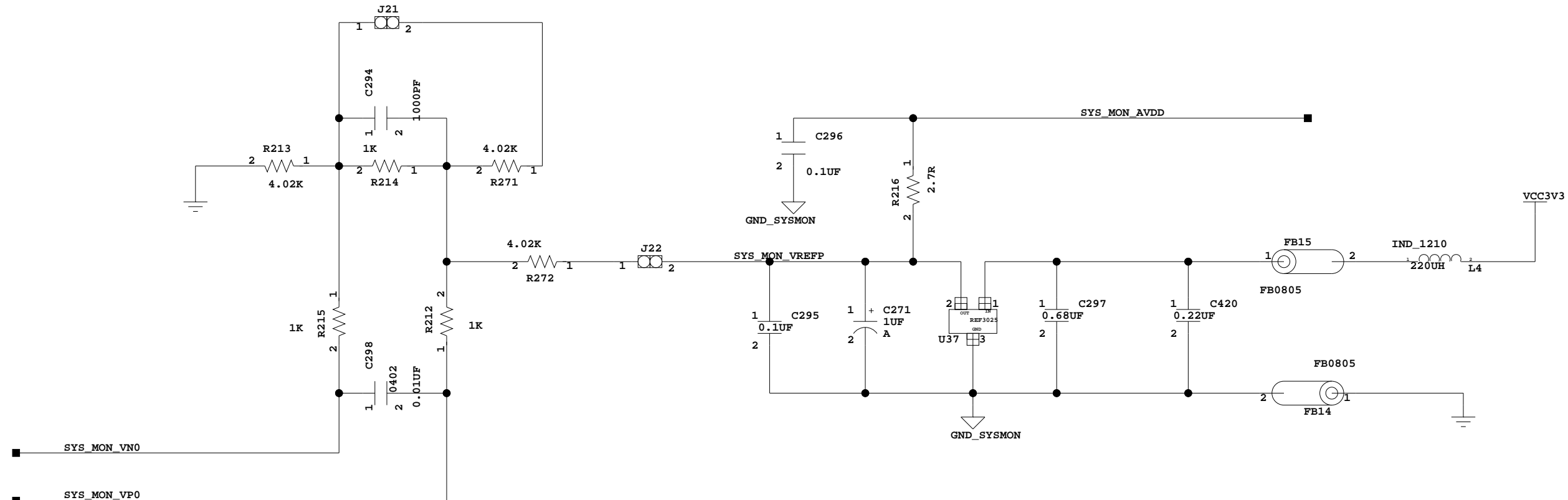
ADV7125
LQFP48



Title:		VGA Codec	
Date:		Ver:	
Sheet Size:	B	Rev:	B
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		Drawn By	BF

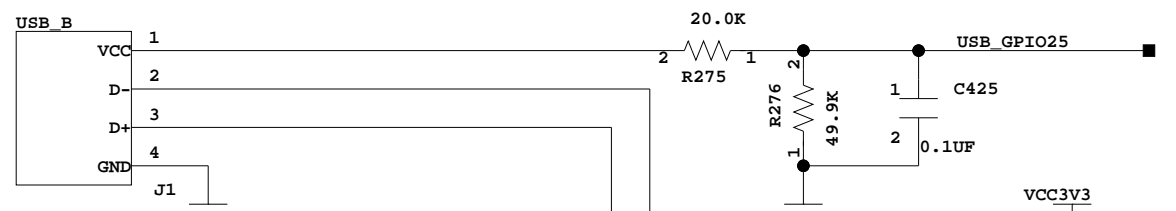


Title:		Audio Codec	
Date:	Sheet Size: B	Ver:	Rev: B
Sheet 17	of 24	Drawn By	BF

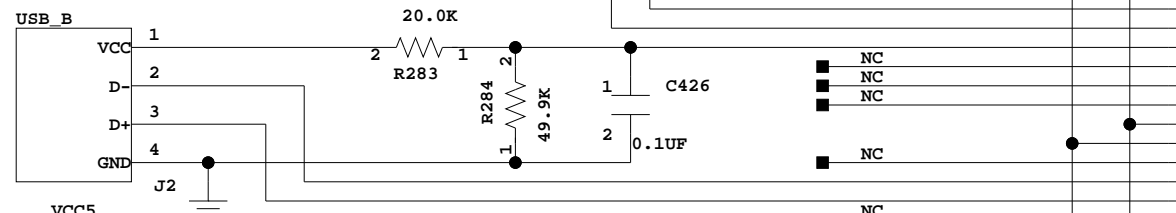


XILINX	
Title: System Monitor DVM Circuit	
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 18 of 24	Drawn By BF

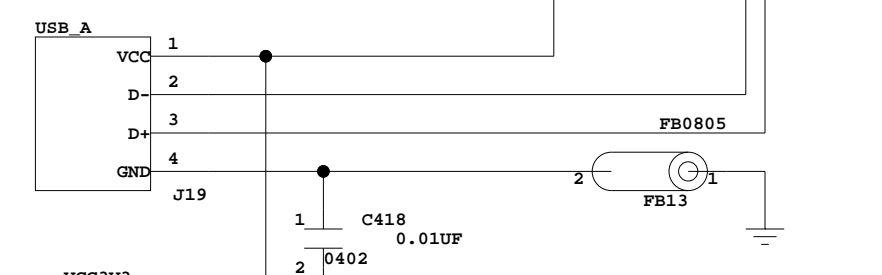
USB Peripheral 2



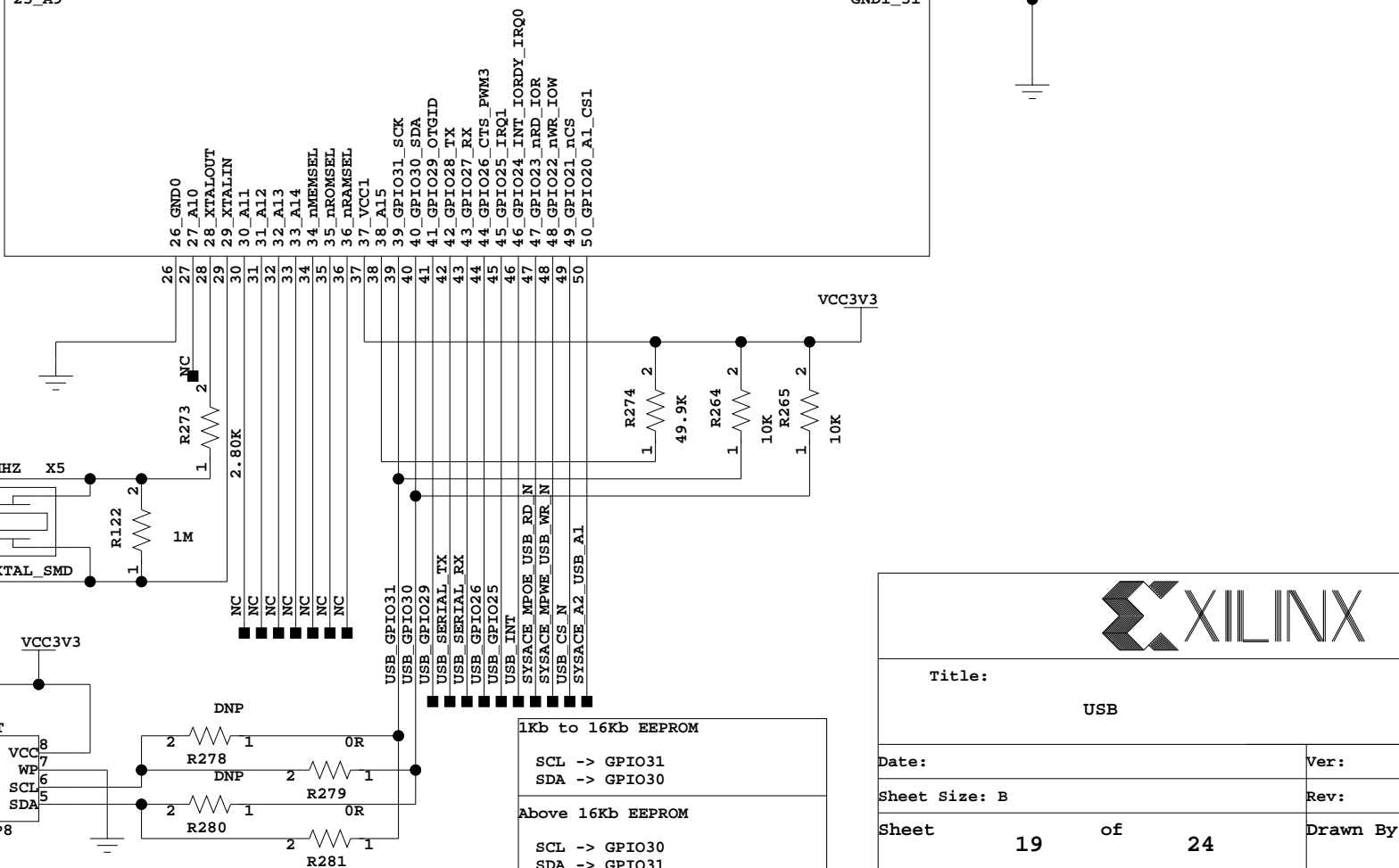
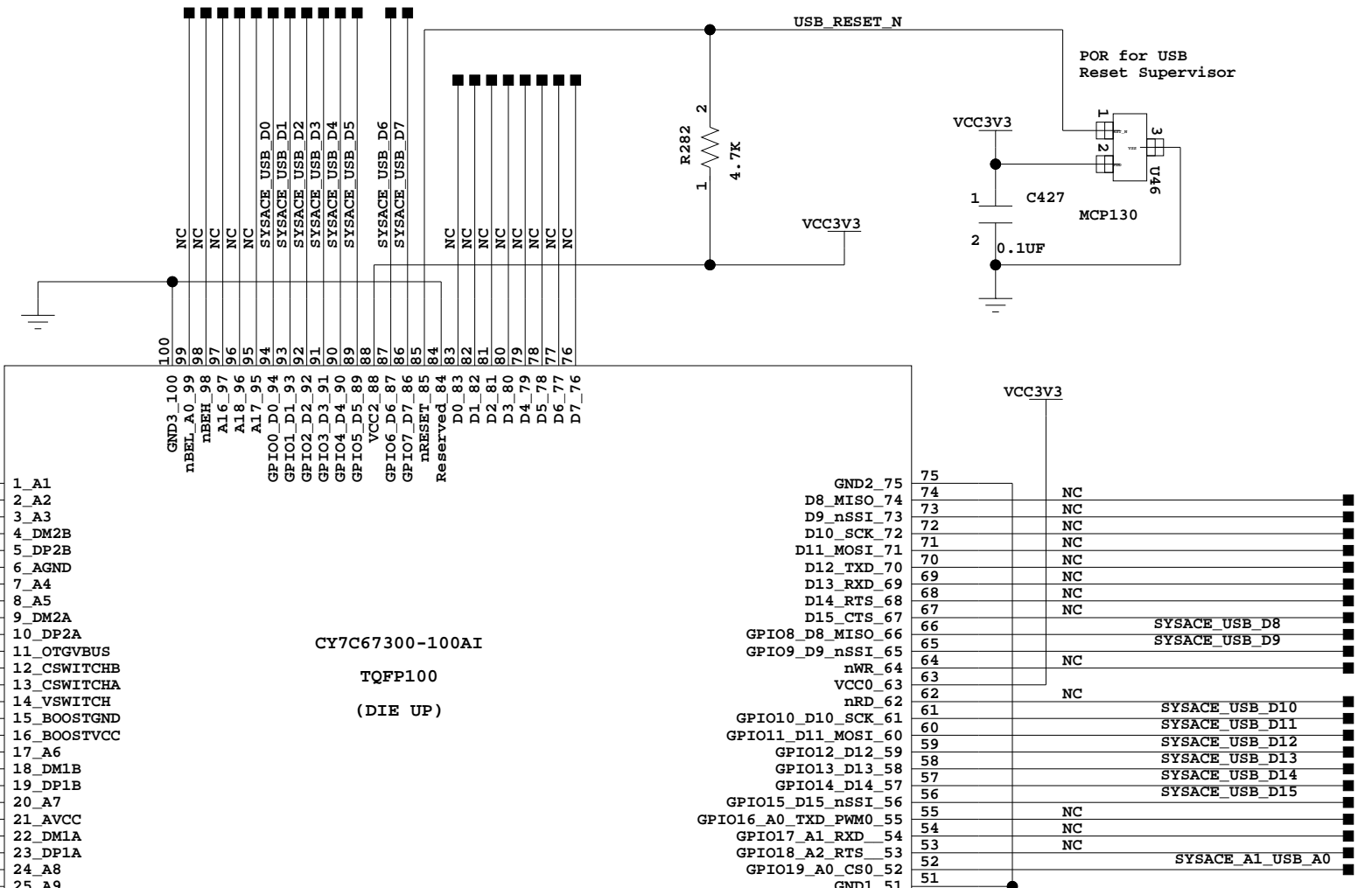
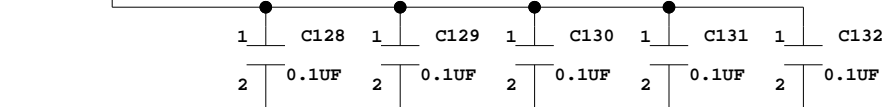
USB Peripheral 1



USB Host 1



Bypass cap for USB chip



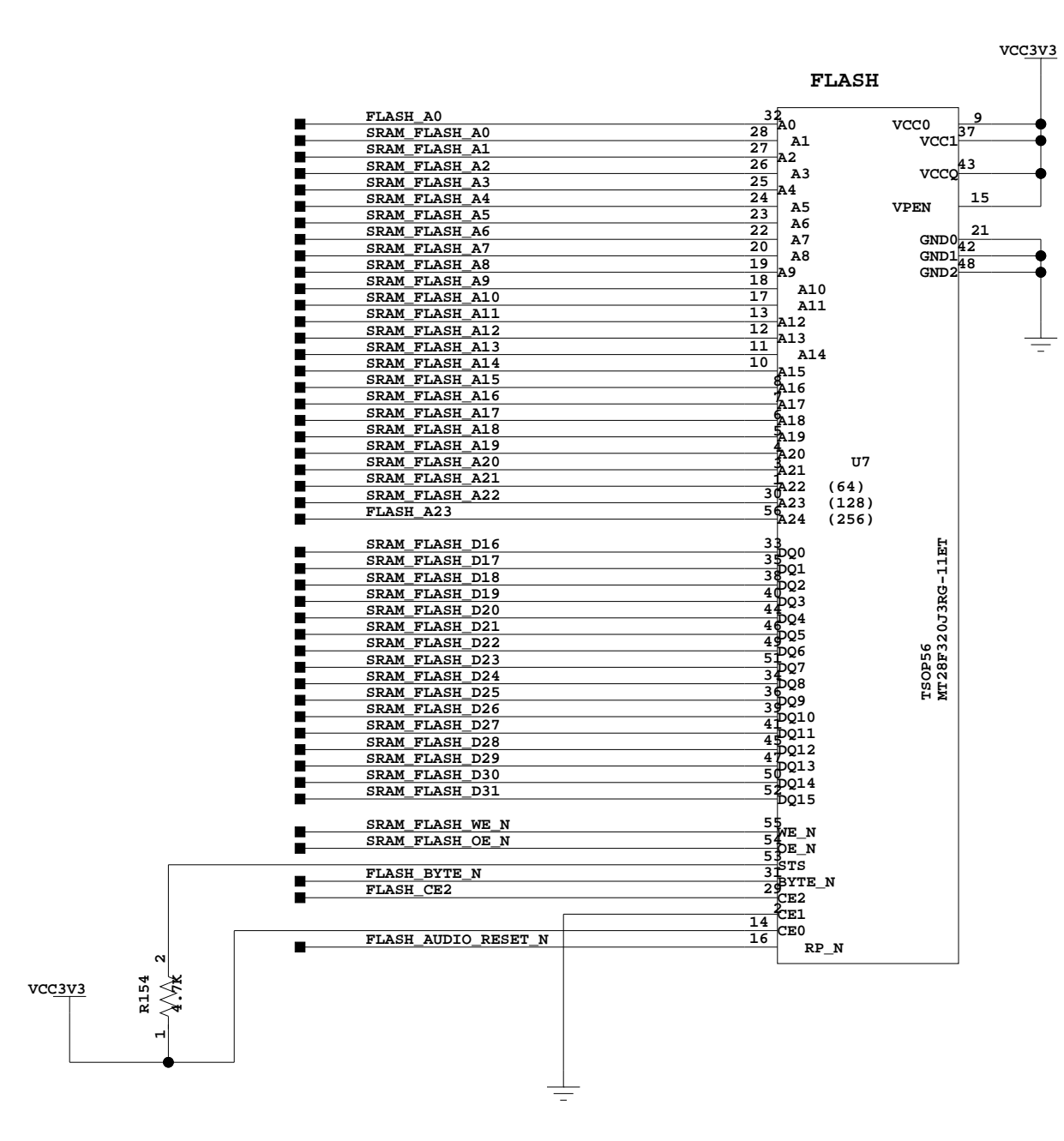
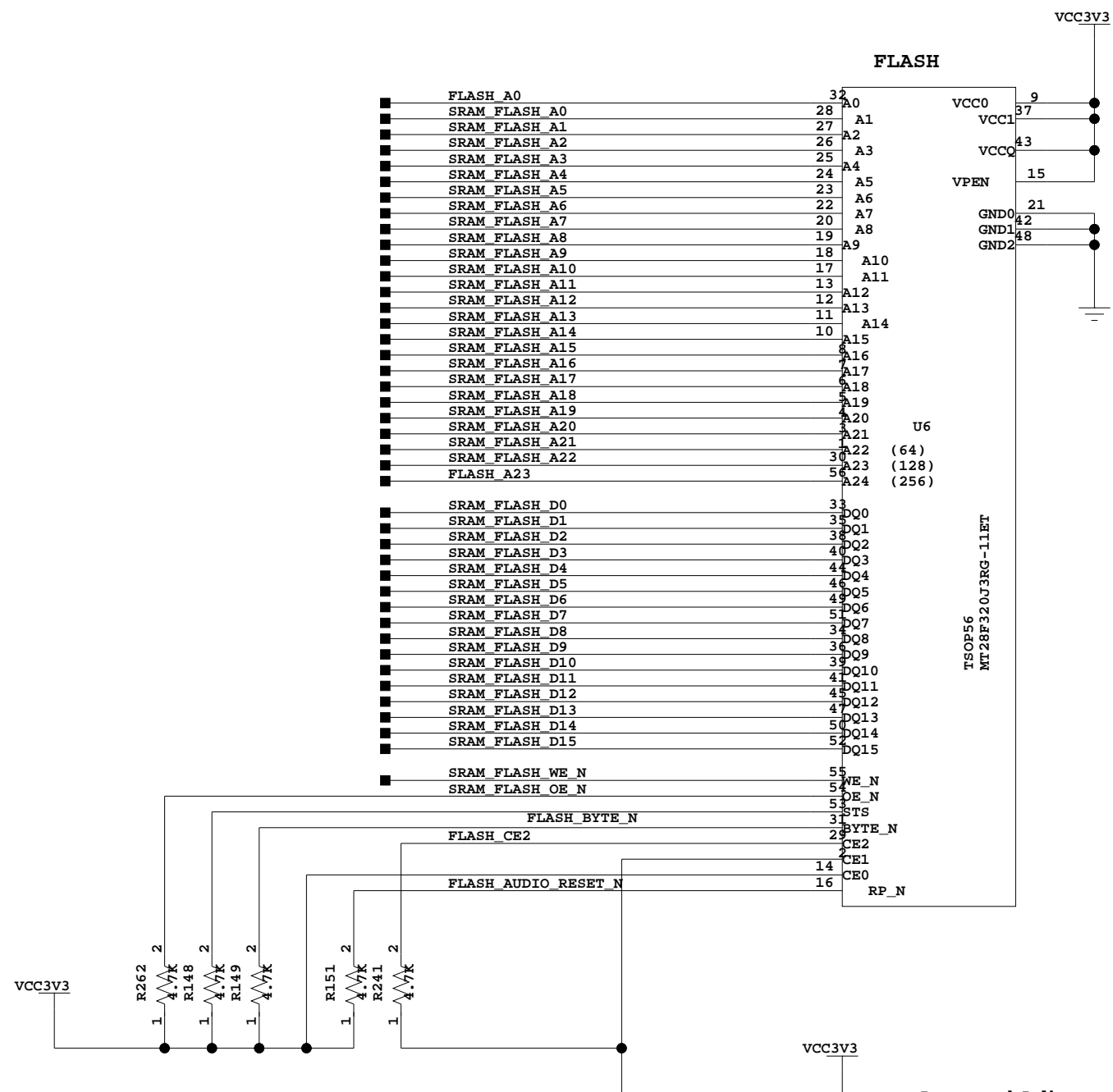
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Title: USB

Date: _____ Ver: _____

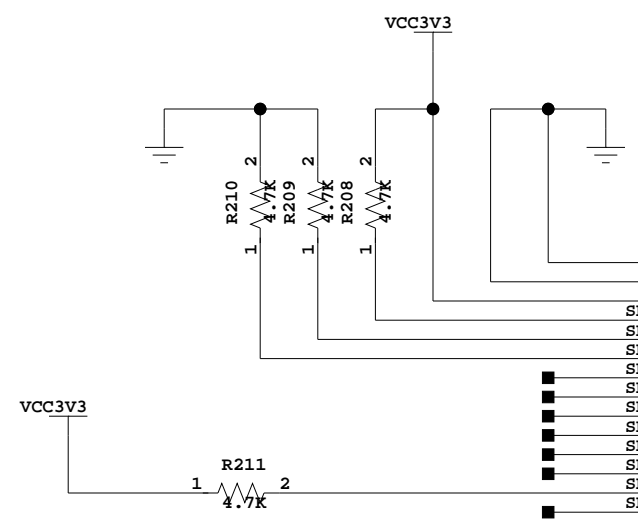
Sheet Size: B Rev: B

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Title:		Flash Memory	
Date:		Ver:	
Sheet Size:	B	Rev:	B
Sheet	20	of	24
Drawn By		BF	

The burst order mode of the SRAM is set to "Linear" by default



87	SRAM CE1_N	98	SRAM CE1_N
92	SRAM MODE	31	SRAM ZZ
97	SRAM ZZ	64	SRAM BW1
98	SRAM BW1	93	SRAM BW0
99	SRAM BW0	94	SRAM BW3
	SRAM BW2	95	SRAM BW2
	SRAM ADV_LD_N	96	SRAM ADV_LD_N
	SRAM FLASH OE_N	85	SRAM FLASH OE_N
	SRAM FLASH WE_N	86	SRAM FLASH WE_N
	SRAM CLK	88	SRAM CLK
		89	SRAM CLK
		37	SRAM FLASH A0
		36	SRAM FLASH A1
		35	SRAM FLASH A2
		34	SRAM FLASH A3
		33	SRAM FLASH A4
		32	SRAM FLASH A5
		44	SRAM FLASH A6
		45	SRAM FLASH A7
		46	SRAM FLASH A8
		47	SRAM FLASH A9
		48	SRAM FLASH A10
		49	SRAM FLASH A11
		50	SRAM FLASH A12
		81	SRAM FLASH A13
		82	SRAM FLASH A14
		83	SRAM FLASH A15
		99	SRAM FLASH A16
		100	SRAM FLASH A17
		84	SRAM FLASH A18
		43	SRAM FLASH A19
		42	SRAM FLASH A20
		39	SRAM FLASH A21
		38	SRAM FLASH A22

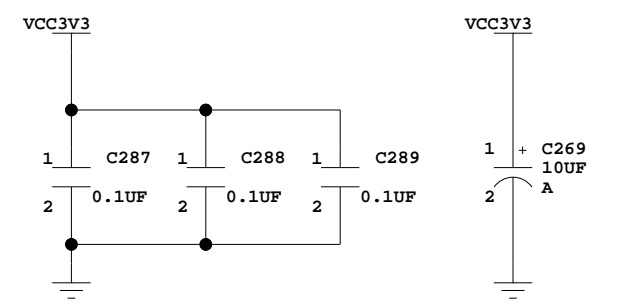
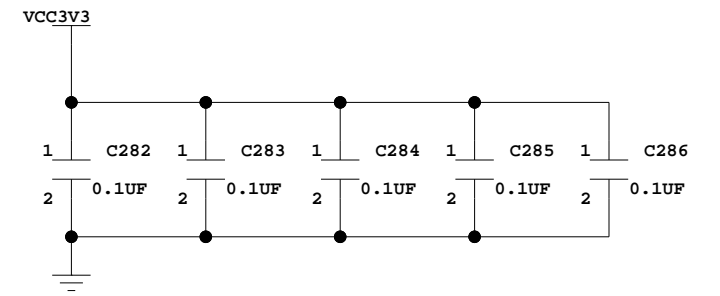
87	CEN_N	66	NC
92	CE3_N	16	NC
97	CE2	14	NC
98	CE1_N	90	NC
31	MODE_31	VSS_90	VSS_90
64	ZZ_64	VSS_76	VSS_76
93	BWA_N	VSS_71	VSS_71
94	BWB_N	VSS_67	VSS_67
95	BWC_N	VSS_60	VSS_60
96	BWD_N	VSS_55	VSS_55
85	ADV/LD_N	VSS_40	VSS_40
86	OE_N	VSS_26	VSS_26
88	WE_N	VSS_21	VSS_21
89	CLK	VSS_17	VSS_17
		VSS_10	VSS_10
		VSS_5	VSS_5
		VDD_91	VDD_91
		VDDQ_77	VDDQ_77
		VDDQ_70	VDDQ_70
		VDD_65	VDD_65
		VDDQ_61	VDDQ_61
		VDDQ_54	VDDQ_54
		VDD_41	VDD_41
		VDDQ_27	VDDQ_27
		VDDQ_20	VDDQ_20
		VDDQ_15	VDDQ_15
		VDDQ_11	VDDQ_11
		VDDQ_4	VDDQ_4

SRAM FLASH D23	47R	5	RP24	4	SRAM FLASH D23 RES
SRAM FLASH D22	47R	6	4	SRAM FLASH D22 RES	
SRAM FLASH D21	47R	7	3	SRAM FLASH D21 RES	
SRAM FLASH D20	47R	8	2	SRAM FLASH D20 RES	
SRAM FLASH D19	47R	1	RP23	1	SRAM FLASH D19 RES
SRAM FLASH D18	47R	5	4	SRAM FLASH D18 RES	
SRAM FLASH D17	47R	6	3	SRAM FLASH D17 RES	
SRAM FLASH D16	47R	7	2	SRAM FLASH D16 RES	
SRAM FLASH D31	47R	8	RP22	1	SRAM FLASH D31 RES
SRAM FLASH D30	47R	5	4	SRAM FLASH D30 RES	
SRAM FLASH D29	47R	6	3	SRAM FLASH D29 RES	
SRAM FLASH D28	47R	7	2	SRAM FLASH D28 RES	
SRAM FLASH D27	47R	8	RP21	1	SRAM FLASH D27 RES
SRAM FLASH D26	47R	5	4	SRAM FLASH D26 RES	
SRAM FLASH D25	47R	6	3	SRAM FLASH D25 RES	
SRAM FLASH D24	47R	7	2	SRAM FLASH D24 RES	

SRAM FLASH D7	47R	5	K?	4	SRAM FLASH D7 RES
SRAM FLASH D6	47R	6	RP17	3	SRAM FLASH D6 RES
SRAM FLASH D5	47R	7	2	SRAM FLASH D5 RES	
SRAM FLASH D4	47R	8	K?	1	SRAM FLASH D4 RES
SRAM FLASH D3	47R	1	RP18	4	SRAM FLASH D3 RES
SRAM FLASH D2	47R	5	3	SRAM FLASH D2 RES	
SRAM FLASH D1	47R	6	2	SRAM FLASH D1 RES	
SRAM FLASH D0	47R	7	K?	1	SRAM FLASH D0 RES
SRAM FLASH D15	47R	8	RP19	4	SRAM FLASH D15 RES
SRAM FLASH D14	47R	5	3	SRAM FLASH D14 RES	
SRAM FLASH D13	47R	6	2	SRAM FLASH D13 RES	
SRAM FLASH D12	47R	7	K?	1	SRAM FLASH D12 RES
SRAM FLASH D11	47R	8	RP20	4	SRAM FLASH D11 RES
SRAM FLASH D10	47R	5	3	SRAM FLASH D10 RES	
SRAM FLASH D9	47R	6	2	SRAM FLASH D9 RES	
SRAM FLASH D8	47R	7	1	SRAM FLASH D8 RES	

SRAM DQP2	47R	1	R287	1	DQPC
SRAM FLASH D31 RES	47R	2		2	DQC
SRAM FLASH D30 RES	47R	3		3	DQC
SRAM FLASH D29 RES	47R	6		6	DQC
SRAM FLASH D28 RES	47R	7		7	DQC
SRAM FLASH D27 RES	47R	8		8	DQC
SRAM FLASH D26 RES	47R	9		9	DQC
SRAM FLASH D25 RES	47R	12		12	DQC
SRAM FLASH D24 RES	47R	13		13	DQC
SRAM FLASH D23 RES	47R	18		18	DQC
SRAM FLASH D22 RES	47R	19		19	DQC
SRAM FLASH D21 RES	47R	22		22	DQC
SRAM FLASH D20 RES	47R	23		23	DQC
SRAM FLASH D19 RES	47R	24		24	DQC
SRAM FLASH D18 RES	47R	25		25	DQC
SRAM FLASH D17 RES	47R	28		28	DQC
SRAM FLASH D16 RES	47R	29		29	DQC
SRAM DQP3	47R	30	R288	1	DQPD
SRAM DQP0	47R	51	R286	2	DQPA
SRAM FLASH D15 RES	47R	52		52	DQA
SRAM FLASH D14 RES	47R	53		53	DQA
SRAM FLASH D13 RES	47R	56		56	DQA
SRAM FLASH D12 RES	47R	57		57	DQA
SRAM FLASH D11 RES	47R	58		58	DQA
SRAM FLASH D10 RES	47R	59		59	DQA
SRAM FLASH D9 RES	47R	62		62	DQA
SRAM FLASH D8 RES	47R	63		63	DQA
SRAM FLASH D7 RES	47R	68		68	DQB
SRAM FLASH D6 RES	47R	69		69	DQB
SRAM FLASH D5 RES	47R	72		72	DQB
SRAM FLASH D4 RES	47R	73		73	DQB
SRAM FLASH D3 RES	47R	74		74	DQB
SRAM FLASH D2 RES	47R	75		75	DQB
SRAM FLASH D1 RES	47R	78		78	DQB
SRAM FLASH D0 RES	47R	79		79	DQB
SRAM DQP1	47R	80	R285	1	DQPB

CY7C1354B TQFP100



Title:		ZBT SRAM	
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SRAM_FLASH_D20_RES	28	28	IO_3_9
SRAM_FLASH_D19_RES	29	29	IO_3_11
SRAM_FLASH_D21_RES	30	30	IO_3_12
SRAM_FLASH_D18_RES	32	32	IO_3_14
SRAM_FLASH_D17_RES	33	33	IO_3_15
SRAM_FLASH_D22_RES	34	34	IO_3_17
CPLD_IO_1	87	87	IO_4_2
CPLD_IO_2	89	89	IO_4_5
CPLD_IO_3	90	90	IO_4_6
SRAM_FLASH_D8_RES	91	91	IO_4_8
SRAM_FLASH_D9_RES	92	92	IO_4_9
SRAM_FLASH_D15_RES	93	93	IO_4_11
SRAM_FLASH_D14_RES	94	94	IO_4_12
SRAM_FLASH_D13_RES	95	95	IO_4_14
SRAM_FLASH_D10_RES	96	96	IO_4_15
SRAM_FLASH_D11_RES	97	97	IO_4_17
SRAM_FLASH_D23_RES	35	35	IO_5_2
SRAM_FLASH_D16_RES	36	36	IO_5_5
FLASH_CE2	37	37	IO_5_6
SRAM_FLASH_D31_RES	39	39	IO_5_8
SRAM_FLASH_D30_RES	40	40	IO_5_9
SRAM_FLASH_D24_RES	41	41	IO_5_11
SRAM_FLASH_D25_RES	42	42	IO_5_12
SRAM_FLASH_D27_RES	43	43	IO_5_14
SRAM_FLASH_D26_RES	46	46	IO_5_15

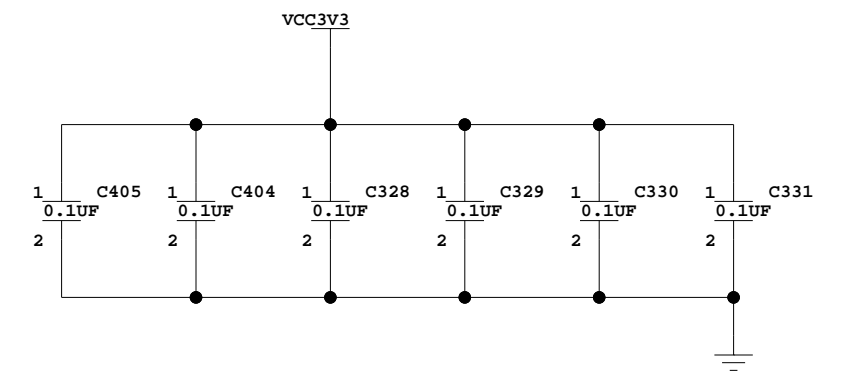
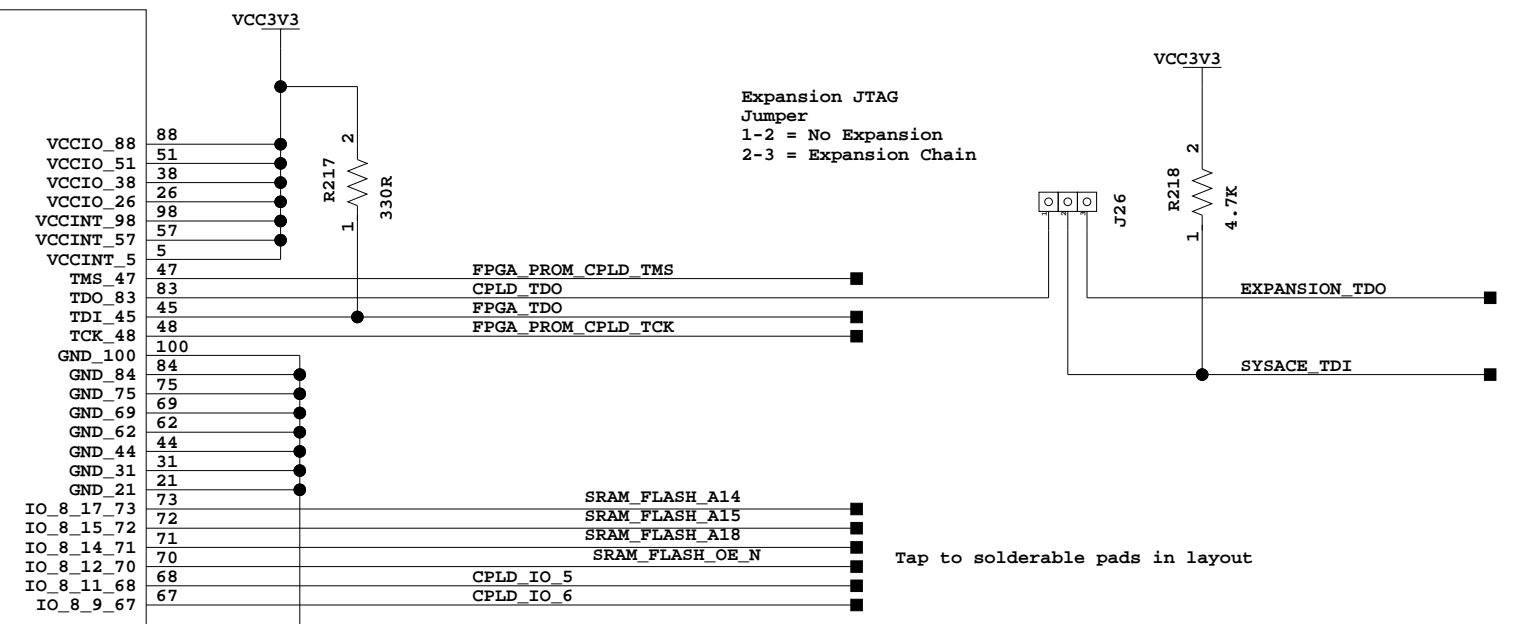
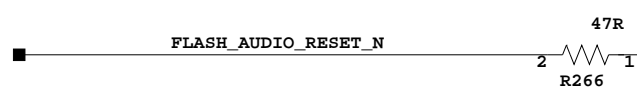
27	PLATFLASH_CPLD_CCLK
25	SRAM_FLASH_A5
24	SRAM_FLASH_A4
23	SYSCLK_100MHZ
10	SRAM_FLASH_A19
9	SYSPACE_CFGADDR2
8	SRAM_FLASH_A6
7	SRAM_FLASH_A7
6	SRAM_FLASH_A8
4	SRAM_FLASH_A9
3	SRAM_FLASH_A10
2	SRAM_FLASH_A11
1	SRAM_FLASH_A12
99	SRAM_FLASH_D12_RES
22	SYSPACE_CLK
20	SRAM_FLASH_A3
19	SRAM_FLASH_A2
18	SRAM_FLASH_A1
17	SRAM_FLASH_A0
16	SRAM_FLASH_A22
15	SRAM_FLASH_A21
14	FPGA_M0
13	SYSPACE_CFGADDR0
12	SYSPACE_CFGADDR1
11	SRAM_FLASH_A20

IO_GCK3_3_8_27	IO_3_6_25	IO_3_5_24	IO_GCK2_3_2_23	IO_2_17_10	IO_2_15_9	IO_2_14_8	IO_2_12_7	IO_2_11_6	IO_GTS2_2_9_4	IO_GTS1_2_8_3	IO_GTS4_2_6_2	IO_GTS3_2_5_1	IO_GSR_2_2_99	IO_GCK1_1_17_22	IO_1_15_20	IO_1_14_19	IO_1_12_18	IO_1_11_17	IO_1_9_16	IO_1_8_15	IO_1_6_14	IO_1_5_13	IO_1_3_12	IO_1_2_11
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XC95144XL
SQ_TQFP100

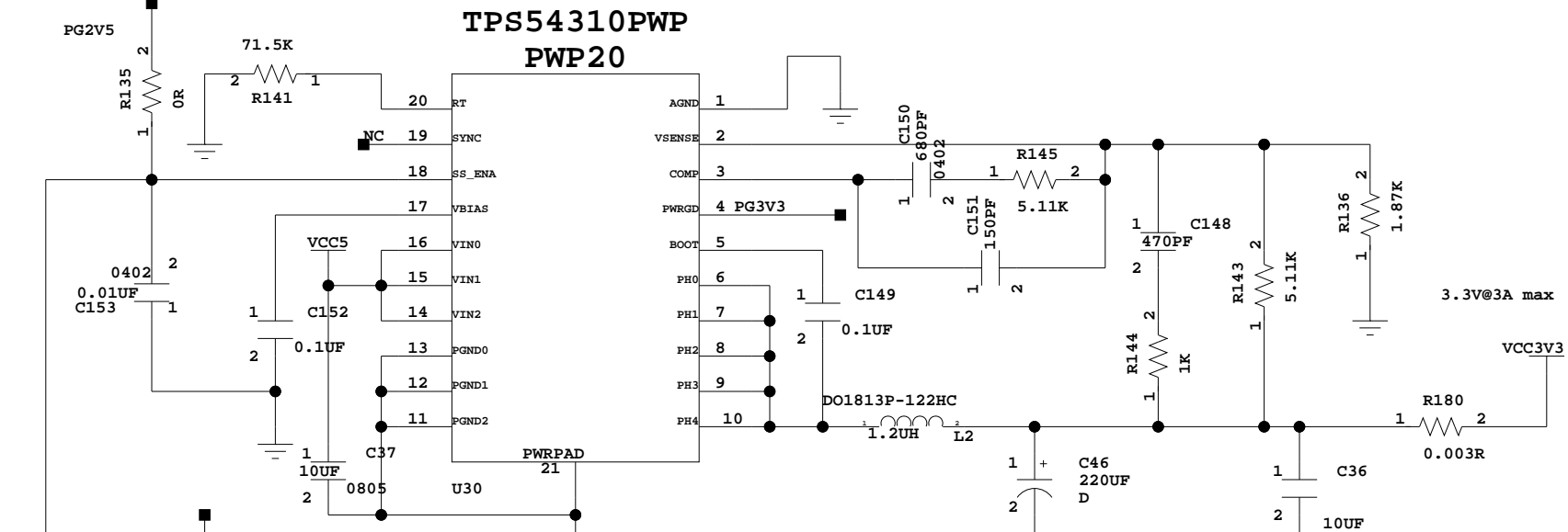
49	SRAM_FLASH_D28_RES
74	SRAM_FLASH_A13
76	SRAM_FLASH_D2_RES
77	SRAM_FLASH_D3_RES
78	SRAM_FLASH_D4_RES
79	SRAM_FLASH_D5_RES
80	SRAM_FLASH_D1_RES
81	SRAM_FLASH_D0_RES
82	SRAM_FLASH_D6_RES
85	SRAM_FLASH_D7_RES
86	FPGA_DOUT_BUSY
50	SRAM_FLASH_D29_RES
52	SRAM_FLASH_A17
53	SRAM_FLASH_A16
54	FPGA_DIN
55	FPGA_DONE
58	FPGA_INIT
59	FPGA_PROG_B
60	FPGA_CS_B
61	FPGA_M1
63	FLASH_A23
64	FPGA_M2
65	FPGA_M0
66	CPLD_PROG
66	CPLD_IO_4

U36

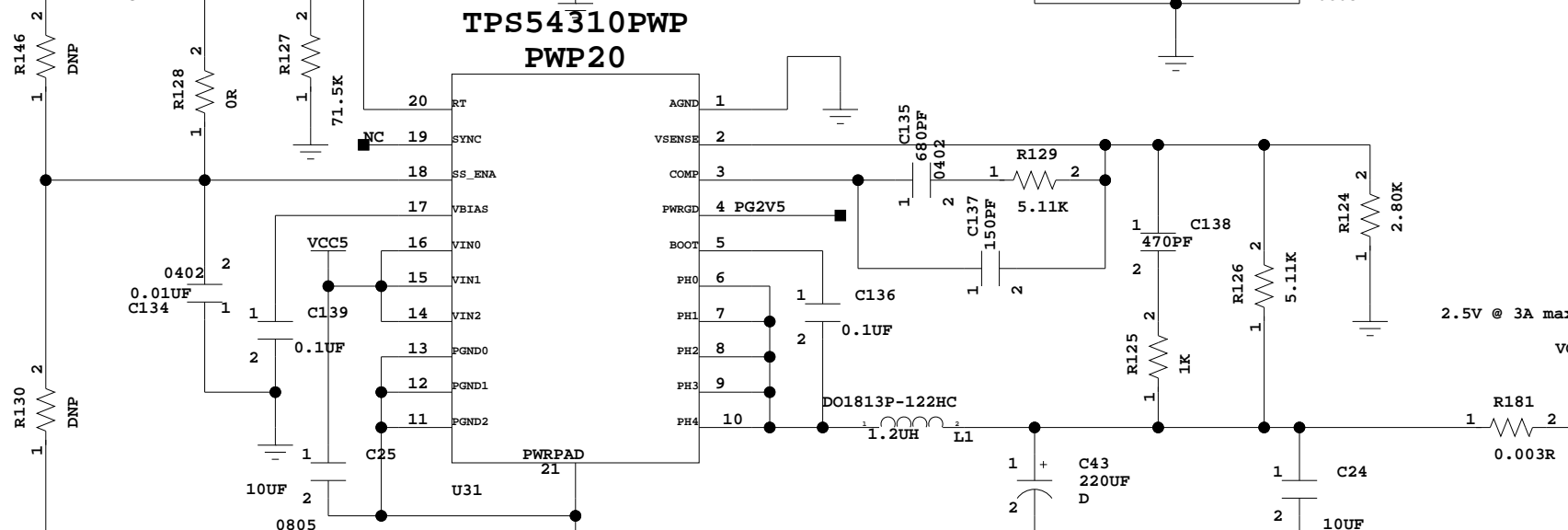


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CPLD for access to Linear Flash	
Date:	Ver:
Sheet Size: B	Rev: B
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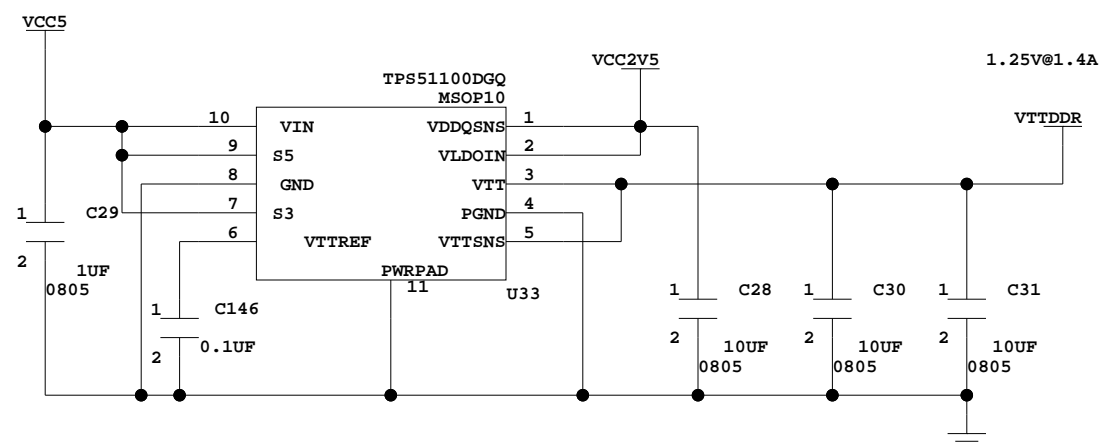
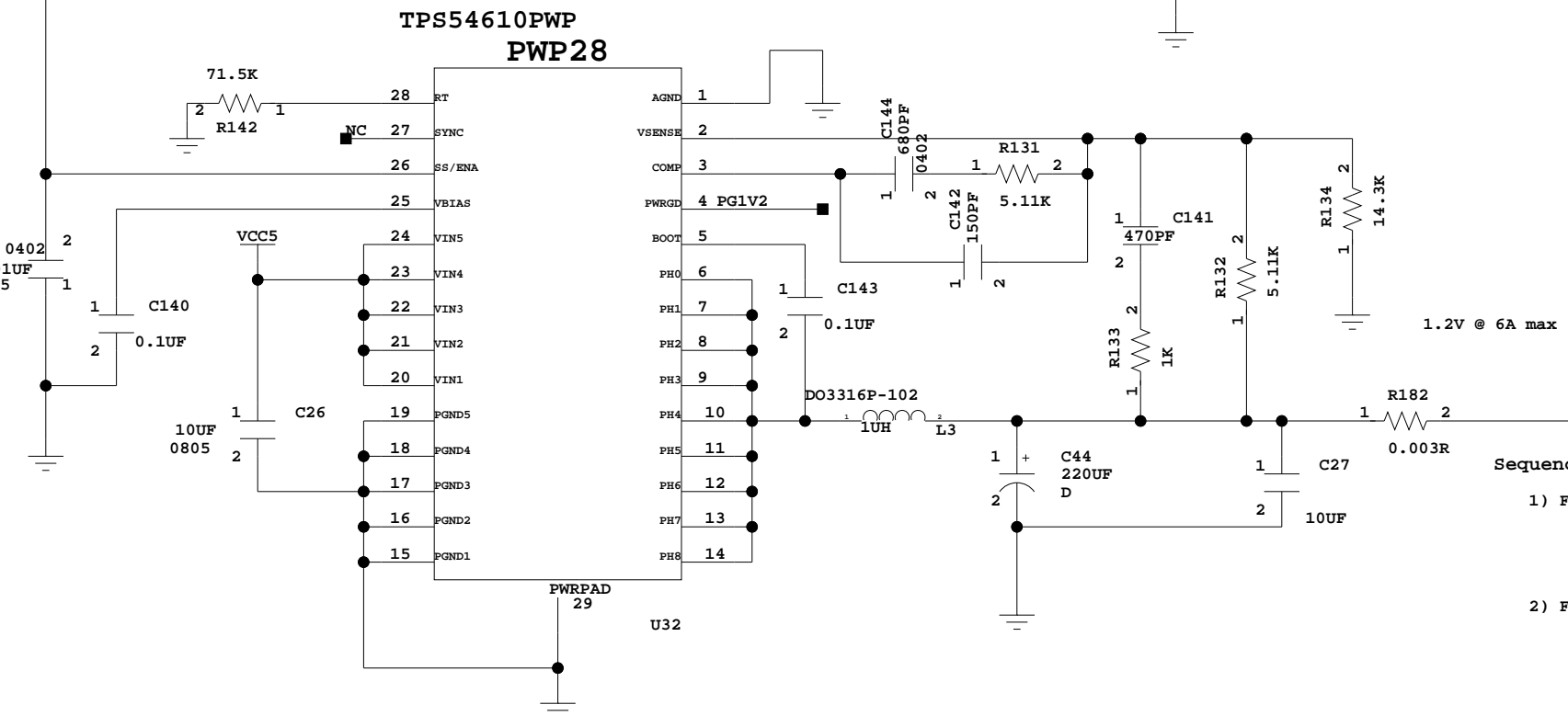
TPS54310PWP PWP20



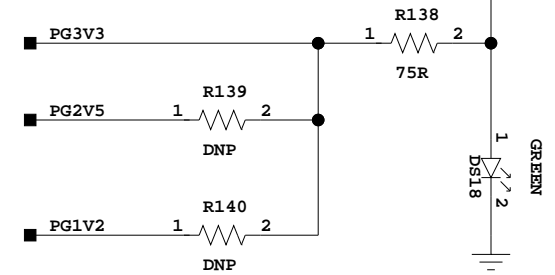
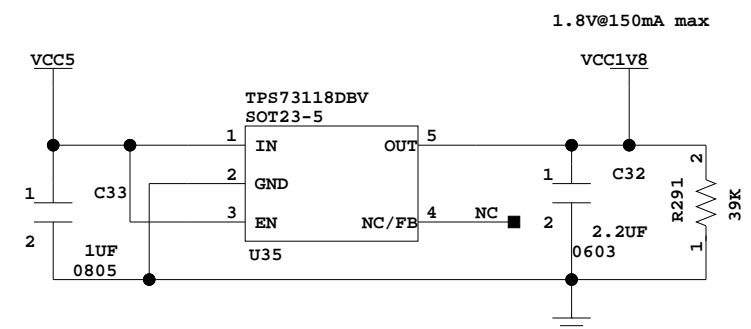
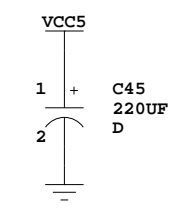
TPS54310PWP PWP20



TPS54610PWP PWP28



4.75V to 5.25V Input

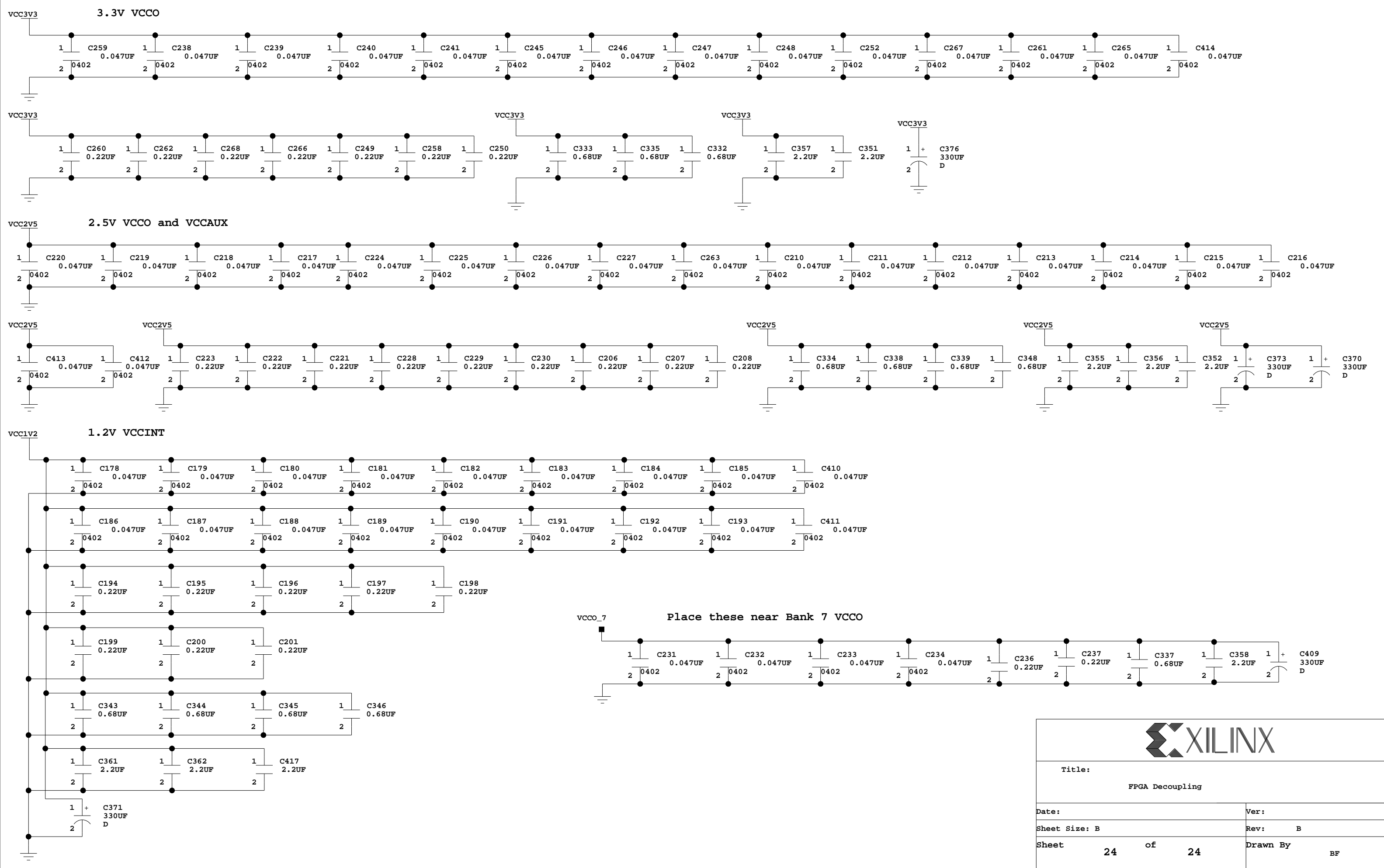


Sequencing Options:

- 1) For sequential startup :
 OPEN R130, R146, R139 & R140
 SHORT R128 & R135
- 2) For ratiometric startup :
 OPEN R128 & R135
 SHORT R130, R146, R139 & R140



Title: Power Supply	
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Title:	
FPGA Decoupling	
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