Best Measure . Best Quality

ZEROPLUS

LAP

使用手冊 User Manual

PC-Based Logic Analyzer LAP-B Series

Index

Preface 3
1 Features of Zeroplus Logic Analyzer 4
1.1 Package Contents 5
1.2 Introduction 7
1.3 Hardware Specifications 9
1.4 System Requirements 11
1.4.1 Operating System Requirements 11
1.4.2 Hardware System Requirements 11
1.5 Device Maintenance and Safety 12
2 Installation 14
2.1 Software Installation 15
2.2 Hardware Installation 17
2.3 Tips and Advice 19
3 User Interface 20
3.1 Menu & Tool Bars 23
3.2 Find Data Value 66
3.3 Statistics Feature 68
3.4 Customize Interface 71
3.4.1 Modify Display Mode 72
3.4.2 Modify Ruler Mode 73
3.4.3 Modify Waveform Height & Correlated Setting 74
3.5 Auto-Save 85
3.6 Color Setting 78
3.6.1 Modify Workaround Color 80
3.6.2 Modify Waveform Color 81
3.7 The Flow of Software Operation 82
4 Introduction to Logic Analysis 83
4.1 Logic Analysis 84
4.2 Bus Logic Analysis 95
4.3 Plug Analysis 98
4.4 Bus Packet List 101
4.5 Bus Analysis 108
4.5.1 Bus Analysis 109
4.5.2 IIC Analysis 113
4.5.2.1 Software Basic Setup of Protocol Analyzer IIC 114
4.5.2.2 Protocol Analyzer IIC Timing Analysis 117
4.5.2.3 Protocol Analyzer IIC Packet Analysis 118
4.5.3 UART Analysis 120
4.5.3.1 Software Basic Setup of Protocol Analyzer UART 121
4.5.3.2 Protocol Analyzer UART Packet Analysis 123
4.5.4 SPI Analysis 125
4.5.4.1 Software Basic Setup of Protocol Analyzer SPI 126
4.5.4.2 Protocol Analyzer SPI Packet Analysis 129
4.5.5 1-WIRE Analysis 132
4.5.5.1 Software Basic Setup of Protocol Analyzer 1-WIRE 137
4.5.5.2 Protocol Analyzer 1-WIRE Packet Analysis 141
4.5.6 HDQ Analysis 142
4.5.6.1 Software Basic Setup of Protocol Analyzer HDQ 142
4.5.6.2 Protocol Analyzer HDQ Packet Analysis 148
4.5.7 CAN2.0B Analysis 149
4.5.7.1 Software Basic Setup of Protocol Analyzer CAN2.0B 149
4.5.7.2 Protocol Analyzer CAN2.0B Packet Analysis 158

4.6 Compression 159
4.6.1 Software Basic Setup of Compression 159
4.7 Signal Filter and Filter Delay 161
4.7.1 Basic Setup of Signal Filter and Filter Delay 161
4.8 Data Contrast 165
4.9 Noise Filter 169
4.9.1 Basic Software Setup of Noise Filter 169
4.10 Refresh Protocol Analyzer 171
4.10.1 Basic Software Setup of Refresh Protocol Analyzer 171
5 Troubleshooting 173
5.1 Installation Troubleshooting 174
5.2 Software Troubleshooting 175
5.3 Hardware Troubleshooting 176
6 FAQ 177
6.1 Hardware 178
6.2 Software 180
6.3 Registration 184
6.4 Technical Information 185
6.5 Others 186
7 Appendix 187
7.1 Hot Keys 188
7.2 Contact Us 190

Preface

This Quick Start Guide is designed to help new and intermediate users navigate and perform common tasks with the Zeroplus Logic Analyzer. Despite its simple packaging and interface, the Logic Analyzer is a sophisticated measurement and analysis tool. It is also a highly sensitive electrical current sensing device. Users must carefully read instructions and procedures pertaining to installation and operation. Any instrument connected to the unit should be properly grounded. A pair of anti-static gloves are strongly recommended when performing a task with the device. To ensure accuracy and consistency of output data, use of the bundled components are strongly recommended.

Users' opinions are very important to Zeroplus. Please contact our engineering team by telephone, fax or email with your questions or feedback. Thank you for choosing the Zeroplus Logic Analyzer.

1 Features of Zeroplus Logic Analyzer

1.1 Package Contents
1.2 Introduction
1.3 Hardware Specifications
1.4 System Requirements
1.5 Device Maintenance and Safety

Objective

In this chapter, users will learn about the package contents, description, hardware specifications, system requirements, and safety issues of the Zeroplus Logic Analyzer. Although this chapter is purely informative, we highly recommend reading this carefully to ensure safety and accuracy when performing any operation with the Zeroplus Logic Analyzer.

1.1 Package Contents

Verify the package contents before discarding packing materials. The following components should be included in your product. For assistance, please contact our nearest distributor.

Table 1-1: Parts List for Retail Packages

Models	**LAP-B(70256) / LAP-B(70256L)**	**LAP-B(702000) / LAP-B(702000L)**	**LAP-B(702000+)**
Logic Analyzer	1	1	1
USB Cable	1	1	1
Power	1	1	1
Probe	X72PCS	X72PCS	X72PCS
Testing Cable	A, B, C, D Port ×4Sets (8Pin×2) Blank×1set (8Pin×1)	A, B, C, D port×4sets (8Pin×2) Blank×1set (8Pin×1)	A, B, C, D port×4sets (8Pin×2) Blank×1set (8Pin×1)
Quick Start Guide	1	1	1
Driver CD	1	1	1
Aluminum Tool Box	1	1	1
Trigger Transmission Channel	selection	selection	selection

* This Driver CD consists of a multilingual software interface program, as well as a multilingual User Manual.

Fig. 1-1: Logic Analyzer

16-Pin x 1
8-Pin x 2

Fig. 1-2: Testing Cable

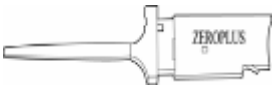


Fig. 1-3: Probe
(varied depending on models)

Fig. 1-4: USB Cable

Fig. 1-5: Quick Start Guide

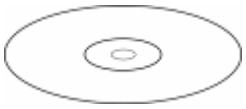


Fig. 1-6: Driver CD

Fig. 1-7: 1-Pin External Clock Cable
(White)

Fig. 1-8: 2-Pin Ground Cable
(Black)

1.2 Introduction

Zeroplus Logic Analyzer LAP-B Series all share the same external features as illustrated in the following figures.

Fig. 1-9: A View of the Zeroplus Logic Analyzer LAP-B Series. See *Fig. 1-11* for detailed information on the **Signal Connectors.**

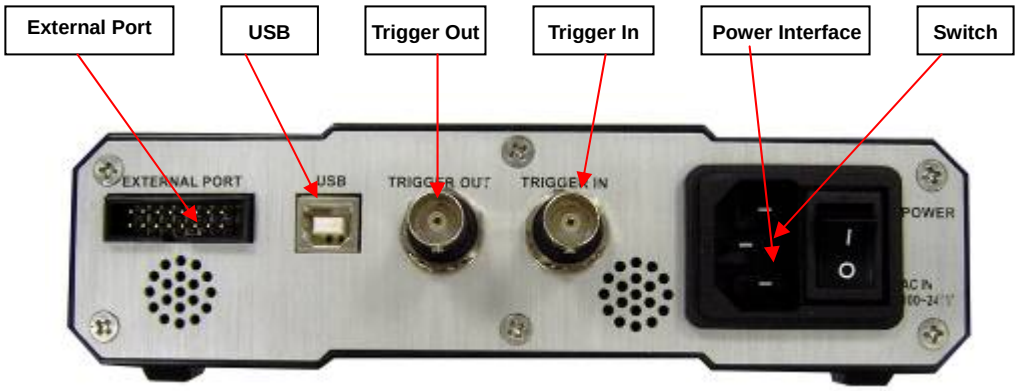


Fig. 1-10: Left Side View of the Zeroplus Logic Analyzer; the power of the Logic Analyzer is drawn from the USB connection.

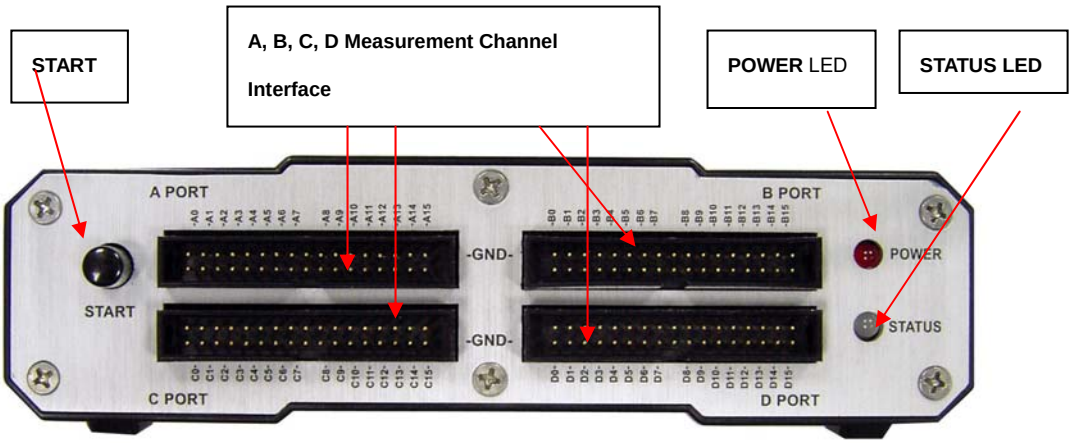


Fig. 1-11: Right Side View of the Zeroplus Logic Analyzer LAP-B Series

Table 1-2: List of Functional Pins in Each Model

Models	LAP-B （70256）	LAP-B （702000)	LAP-B （70256L）	LAP-B （702000L）	LAP-B （702000+）
Port A (**A00~A15**)	√	√	√	√	√
GND	√	√	√	√	√
Port B (**B00~B15**)	√	√	√	√	√
GND	√	√	√	√	√
Port C (**C00~C15**)	√	√	√	√	√
GND	√	√	√	√	√
Port D (**D00~D15**)	√	√	√	√	√
GND	√	√	√	√	√
C0	√	√	√	√	√
C1	√	√	√	√	√
C2	√	√	√	√	√
T1	√	√	√	√	√
T2	√	√	√	√	√
GND	√	√	√	√	√
TRIGGER IN(T0)	√	√	√	√	√
TRIGGER OUT	√	√	√	√	√

Table 1-3: Definitions and Functions of Pins for Advanced Models

C0	External Clock	When using the External Clock for sampling , it receives the external clock .
C1	External Clock	When using the External Clock for sampling , it receives the external clock .
C2	External Clock	When using the External Clock for sampling , it receives the external clock .
T1	Trigger In	When using the External Clock Signal, it receives the external signal.
T2	Trigger In	When using the External Clock Signal, it receives the external signal.
TRIGGER IN(T0)	Trigger In	When using the External Clock Signal, it receives the external signal.
TRIGGER OUT	Trigger Out	The trigger out signal is used for outputting the trigger signal.

1.3 Hardware Specification

Table 1-4：Hardware Specifications of LAP-B Series

Items\Type		**LAP-B (70256) / LAP-B (70256L)**		**LAP-B(702000)/ LAP-B(702000L)**		**LAP-B(702000+)**		
Channel Mode		_		_		**70-Channel Mode**	**32-Channel Mode**	**16-Channel Mode**
Operating		Win2000/XP/Vista						
Interface		USB 2.0(1.1)						
Power		AC100~240V, 50~60Hz						
Sample Rate	Internal Clock (Timing Mode)	1Hz~400MHz		1Hz~400MHz		1Hz~ 333MHz	100MHz~ 500MHz	200MHz~ 1000MGHz
	External Clock (State Mode)	Max 150MHz		Max 150MHz			N/A	N/A
	Frequency Width	100MHz		100MHz		150MHz		
Memory	Memory	17.5Mbits		140Mbit				
	Memory Depth	256Kbits		2Mbits			4Mbits	8Mbits
Trigger	Trigger Channel	70CH		70CH			32CH	16CH
	Trigger Condition	Pattern/Edge /Wide/AND/OR						
	Pre-Trigger/ Post-Trigger	N/A						
	Waveform Trigger Width	YES						
	Trigger Level	9 Level		16 Level				
	Trigger Count	1~65535						
Threshold Voltage	Working Range	-6V~+6V						
	Accuracy	±0.1V						
Protocol Analyzer (Keep Increasing)	IIC	Free						
	UART	Free						
	SPI	Free						
	1-WIRE	Free	Option	Free	Option	Free		
	CAN 2.0B	Free	Option	Free	Option	Free		

	HDQ	Free	Option	Free	Option	Free			
	7-SEGMENT LED	Free							
Software Functions	Operating Interface Language	Chinese(Si)/ Chinese(Tr)/ English							
	Time Base Range	5ps~10Ms							
	Vertical Sizing	1~5.5							
	Filter Delay	YES		YES			N/A		N/A
	Data Compression	128Kbits x 2^{32}		1Mbits x 2^{32}			N/A		N/A
	Width Display	YES		YES					
	Trigger Page	1~8192Page		1~8192Page			N/A		N/A
	Signal Filter Bar	YES		YES			N/A		N/A
	Trigger Delay	N/A							
	Infinite Increase Spacer Bar	YES							
	Automatic Zoom In of Spacer Bar	YES							
	Automatic Software Update	YES							
	Data Range Selectable	YES							
	Data Count	YES							
	Bus Inquiry and Counter	YES							
Safety Certification		FCC/CE							

1.4 System Requirements

This section discusses basic operating system and hardware requirements for the Logic Analyzer. Software and hardware capabilities may vary depending on PC configuration; this manual assumes proper installation of a supported operating system as listed below.

1.4.1 Operating System Requirements

Table 1-5: Operating System Requirements of LAP-B Series

	Support	Non-support
Operating System Name	● Windows 2000 (Professional, Server Family) ● Windows XP (Home, Professional Editions 32-Bit version) ● Windows VISTA (32-Bit and 64-Bit version)	● Windows NT 4.0 (Workstation & Server, Service Pack 6) ● Windows Server 2003

1.4.2 Hardware System Requirements

Table 1-6: Hardware System Requirements of LAP-B Series

Hardware Name	Lowest Configuration	Recommended Configuration
CPU	166 MHz	900 MHz
Memory	64MB	256MB
Display Devices	VGA Display Capability with 1024x768 resolution or higher.	VGA Display Capability with 1024x768 resolution or higher.
Hard Drive	At least 100MB available space	At least 100MB available space
USB	USB1.1 supported	USB2.0 supported

1.5 Device Maintenance and Safety

Follow these instructions for proper operation and storage of the Logic Analyzer.

Table 1-7：General Advice

Cautions	• Do not place heavy objects on the Zeroplus Logic Analyzer. • Avoid hard impacts and rough handling. • Protect the Logic Analyzer from static discharge. • Do not disassemble the Zeroplus Logic Analyzer; this will void the warranty and could affect its operation.
Cleaning	• Use a soft, damp cloth with a mild detergent to clean. • Do not spray any liquid on the Zeroplus Logic Analyzer or immerse it in any liquid. • Do not use harsh chemicals or cleaners containing substances such as benzene, toluene, xylene or acetone.

Table 1-8：Electrical Specifications

Items	Minimum	Typical	Maximum
Working Voltage	DC 4.5 V	DC 5.0 V	DC 5.5 V
Current at Rest			200 mA
Current at Work			400 mA
Power at Rest			1 W
Power at Work			2W
Error in Phase Off*			± 1.5 nS
V_{input} of Testing Channels			± DC 30 V
$V_{Reference}$	DC -6		DC +6 V
Input Resistance		500KΩ/10pF	
Working Temperature	5°C		70°C
Storage Temperature	-40°C		80°C

* Refer to the User Manual for error analysis calculation.

Table 1-9：Operating Environment

WARNING	• Avoid direct sunlight • Use in a dust free, non-conductive environment (see Note) • Relative Humidity: < 80% • Altitude: < 2000m • Temperature: 0 ~ 40 degrees C This is a Class A product which may cause radio interference in a domestic environment.
	Note: EN 61010-1: 2001 specify degrees of pollution and their requirements. Logic Analyzer falls under Level 2. Pollution refers to 'addition of foreign matter, solid, liquid or gaseous (ionized gases), which may produce a reduction of dielectric strength or surface resistivity'. Pollution Degree 1: No pollution or only dry, non-conductive pollution occurs. This pollution has no effect. Pollution Degree 2: Normally only non-conductive pollution occurs. Occasionally, however, temporary conductivity caused by the condensation must be expected. Pollution Degree 3: Conductive pollution occurs or dry, non-conductive pollution which becomes conductive due to the condensation occurs. In such conditions, the equipment is normally protected against exposure to direct sunlight, precipitation and wind, but neither temperature nor humidity is controlled.
Storage Environment	Relative Humidity: < 80% Temperature: 0 ~ 50 degrees C

Conclusion

After reading this section, users should have a basic grasp of the Logic Analyzer. A complete understanding of the section, **Device Maintenance and Safety**, is a critical prerequisite of any further operation as presented in the User Manual.

2 Installation

2.1 Software Installation
2.2 Hardware Installation
2.3 Tips and Advice

Objective

This chapter describes installation of the Logic Analyzer hardware and software. Software installation steps must be followed precisely to ensure successful installation.

2.1 Software Installation

In this section, users will learn how to install the software interface and drivers. As with proper installation of many USB devices, the Logic Analyzer application and driver software must be installed prior to the connection of the hardware. The following steps illustrate an installation of a Zeroplus **LAP-B（70256）**Logic Analyzer. The other four models mentioned in Chapter 1 would follow the identical procedures.

Step 1. Insert the driver CD-ROM in the PC CD drive.

Step 2. Execute the installation program. Go to the START menu, click **START**, click **Run**, click **Browse**, select **Setup.exe** file in the appropriate model folder and then click **OK**. It is recommended that all other programs are closed while the installation proceeds.

Step 3. Choose the desired language.

Step 4. Click **Next** to proceed with the Install Wizard.

Step 5. Select "**I accept the term in this license agreement** ", and click **Next**.

Step 6. Enter User and Organization Name.

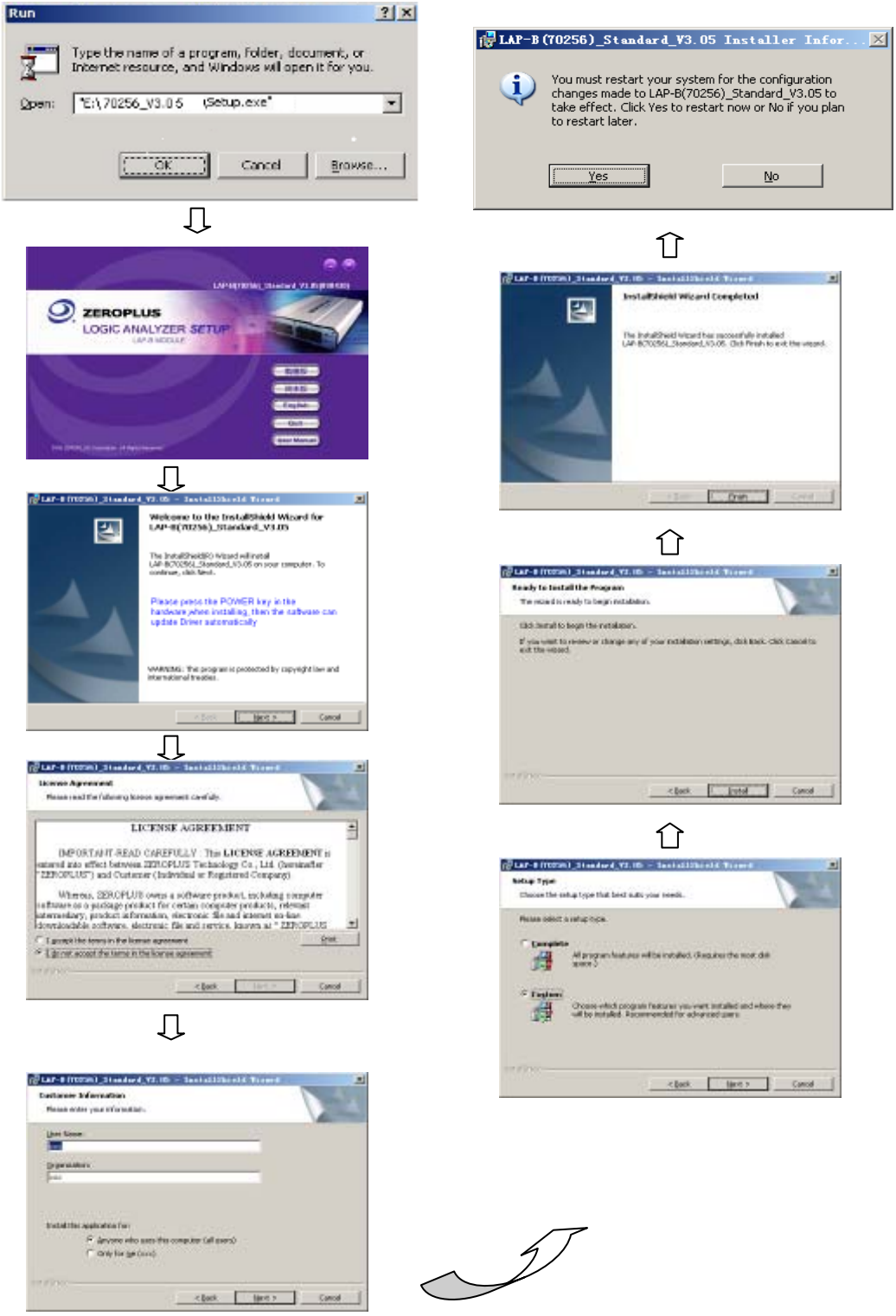
Step 7. Choose the setup type. We recommend **Complete** for most users.

Step 8. Click **Install** to confirm settings and begin the actual installation.

Step 9. Click **Yes** to acknowledge the Microsoft Digital Signature message and continue the installation.

Step 10. Click **Finish** to complete the installation.

Step 11. Click **Yes** to restart the PC.


Run
Type the name of a program, folder, document, or Internet resource, and Windows will open it for you.
Open:
OK
Cancel
Browse...
ZEROPLUS
LOGIC ANALYZER SETUP
LAP-B(70256)_Standard_V3.05 Installer Infor...
You must restart your system for the configuration changes made to LAP-B(70256)_Standard_V3.05 to take effect. Click Yes to restart now or No if you plan to restart later.
Yes
No
LICENSE AGREEMENT

2.2 Hardware Installation

Hardware Installation simply involves in connecting the Logic Analyzer to your computer with the included USB Cable as shown in Figures 2-4 and 2-5.

1. Plug the fixed end of the cables into the LA (Fig.2-1).

Fig. 2-1

2. Plug the loose ends into the connectors on the circuit board to be analyzed (Fig.2-2).

Note: The following sequence must be observed when plugging the connectors into the circuit board: Such as A0 = Brown, A2 = Red, A3=Orange and so on.

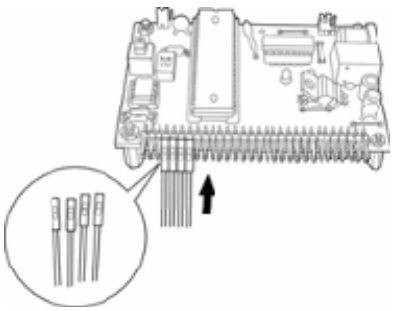


Fig. 2-2

3. The circuit board must be grounded to the Logic Analyzer with the black Ground Cable (Fig.2-3).

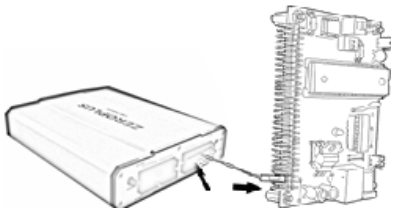


Fig. 2-3

Step 1 - Plug the thin male end of the USB cable into the laptop or PC.
Step 2 - Plug the square female end into the Logic Analyzer.

4. Plug the square end of the USB cable into the Logic Analyzer (Fig. 2-4).

Fig. 2-4

5. Plug the thin end into the computer (Fig. 2-5).

Fig. 2-5

At this point, the computer should be able to detect the Logic Analyzer and finalize the installation for hardware connection. For further information, refer to the Troubleshooting and Frequently Asked Questions (FAQ) chapters in the User Manual.

Fig. 2-6: An Assembly of Laptop, Logic Analyzer, and a Testing Board

2.3 Tips and Advice

1. When testing a circuit board, make sure that the internal sampling frequency (within the Logic Analyzer) is at least four times higher than the external board frequency.
2. If the signal connector does not work well with the pins on the test board, try using the supplied probes.

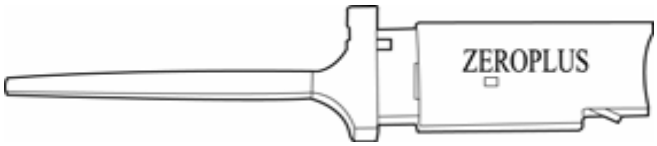
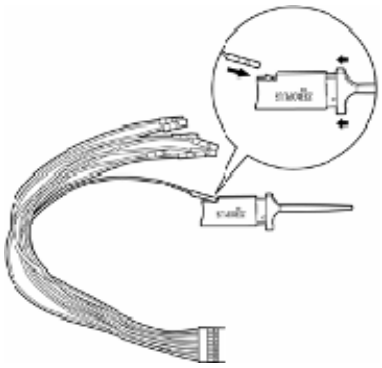
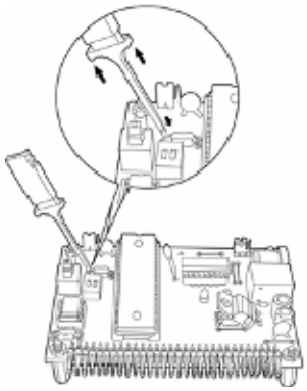


Fig. 2-7: Probes Supplied with the Zeroplus



3.
3-1. Take the loose end of the cable and insert it into the clip.

Fig. 2-8



3-2. Compress the probe as shown to reveal 2 metal prongs (Fig.2-8).
3-3. Place the metal prongs on a metal connector on the testing board and release the fingers so that the prongs can grip the metal connector (Fig.2-9).

Fig.2-9

4. The Logic Analyzer will connect to the **Zeroplus** server for software updates if an internet connection is available.
5. Unwanted signals can be filtered out using the **Signal Filter** or **Filter Delay** functions.
6. When measuring for a long period, **Compression** makes memory more efficient.
7. Trigger condition depends on the test board. If triggering does not work well, try narrowing the trigger conditions and optimize them repeatedly.
8. If a test board has a lower frequency than Logic Analyzer, sample signals according to the external clock.
9. When sampling from an external clock, filter extra signals with the Signal Filter function.
10. Unused channels may be removed from the **Bus/Signal** display using **Bus/Signal** (Menu) ➔ Channels Setup.

3 User Interface

3.1 Menu & Tool Bars
3.2 Find Data Value
3.3 Statistics Feature
3.4 Customize Interface
3.5 Auto-Save
3.6 Color Setting
3.7 The Flow of Software Operation

Objective

Chapter 3 presents detailed information on the Logic Analyzer software interface in four sections: **Menu Bar**, **Tool Bar**, **Statistical Function** and **Interface Customization**.

Basic Layout

The layout of the Logic Analyzer software interface can be divided into nine sections as shown in the following figure.

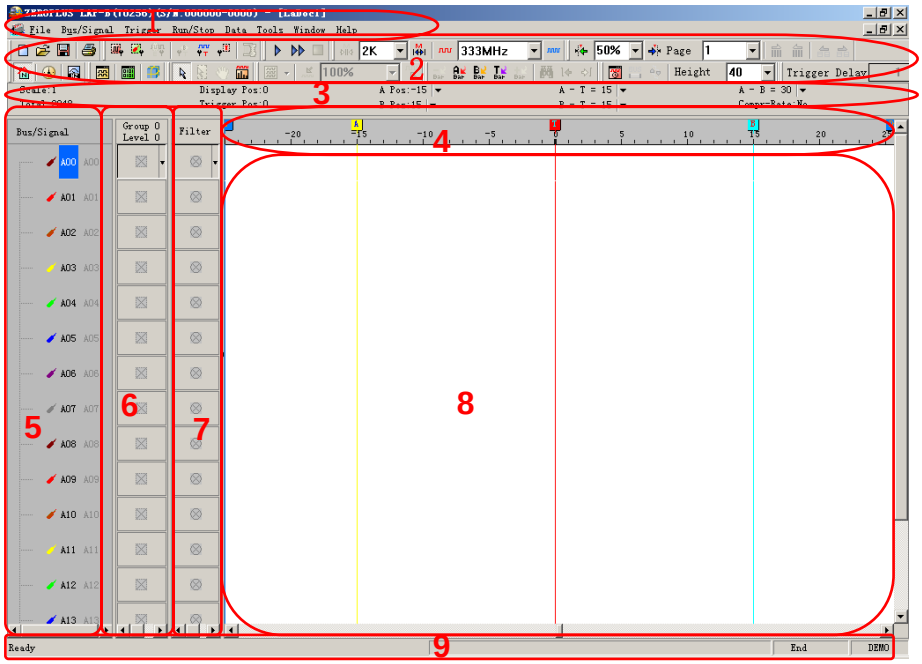


Fig 3-1 – Software Interface

1. **Menu Bar**

   All operations are performed directly from the menu bar, including **configure label**, **rename**, **execute** and **stop**. Pull-down menus allow easy navigation through the measurement pane.

2. **Tool Bar**

   The tool bar is the graphical user interface which can make you work with some of the more common applications. From these icons, you can change settings and operate the Logic Analyzer easily.

3. **Information Bar**

   The Information Bar displays information about the grids in the waveform. For example: Address, Time, Frequency, Trigger Bar, A Bar, B Bar and other Bars. Details of the labels are below:

Scale -	Define the acquisition clock that controls the data sampling.
Total -	The period of time when Logic Analyzer captures data.
Display Pos -	The middle tip means the middle position of the waveform.
Trigger Pos -	Trigger position.
A Pos -	The main function is setting A Bar or the others.
B Pos -	The main function is setting B Bar or the others.
A-B -	Press the under arrow to exchange and become the other Bars. Moreover, you also can execute this function from the other Bars.

4. **Ruler (Waveform Display / Listing Display)**

   Ruler shows the time position of the waveform shown in the waveform display area or the listing display area.

5. **Bus/Signal (Waveform Display / Listing Display)**

   Edit names of the measured channels; color shown matches the trace color.

6. **Trigger Column**

   Trigger Column allows users to adjust signal trigger conditions.

7. Filter Column

Filter Column allows users to set Bus or signal Filter conditions.

8. Display Area

Acquired data is displayed as a waveform or in a list format.

Waveform Display

This interface shows the digital signals. When the signal is logic "0", the waveform will be displayed as ▬. If the signal is logic "1", the waveform is as ▔. An unknown signal waveform is displayed in gray between the high and low levels as ▭. There are seventy channels in LAP-B(70256), LAP-B(70256L), LAP-B(702000), LAP-B(702000L) and LAP-B(702000+). But when the LAP-B(702000+) is in the 16-Channel Mode, the number of channels will be 16; when the LAP-B(702000+) is in the 32-Channel Mode, the number of channels will be 32.

Listing Display

This interface shows the digital signals as 1 and 0. Logic 1 is displayed as "1" and logic 0 is displayed as "0".

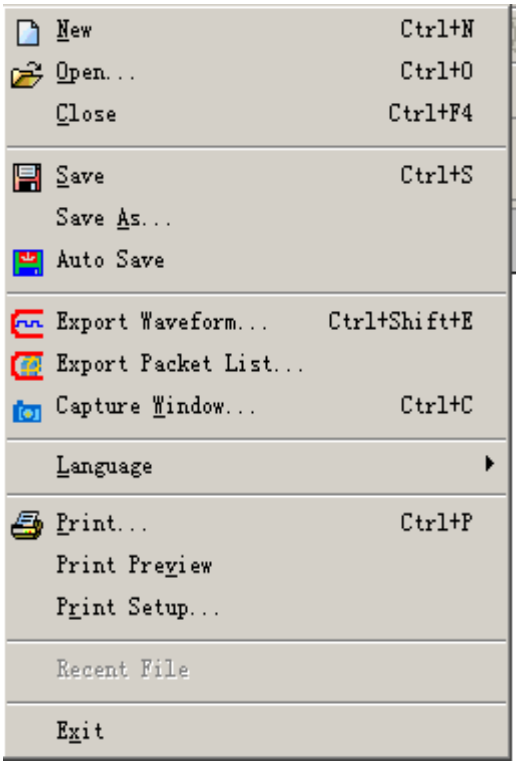
9. Status Area

Display Logic Analyzer status. The function name is also indicated here.

3.1 Menu & Tool Bars

Section 3.1 presents detailed information on the eight menu and thirteen tool items shown in the Menu Bar. The eight menu items are **File**, **Bus/Signal**, **Trigger**, **Run/Stop**, **Data**, **Tools**, **Window** and **Help**. The thirteen tool items are **Standard**, **Trigger**, **Run/Stop**, **Sampling**, **Trigger Content Set**, **Display Mode**, **Windows**, **Mouse Pattern**, **Zoom**, **Data**, **Show Time/Height**, **Trigger Delay** and **Font Size**.

File

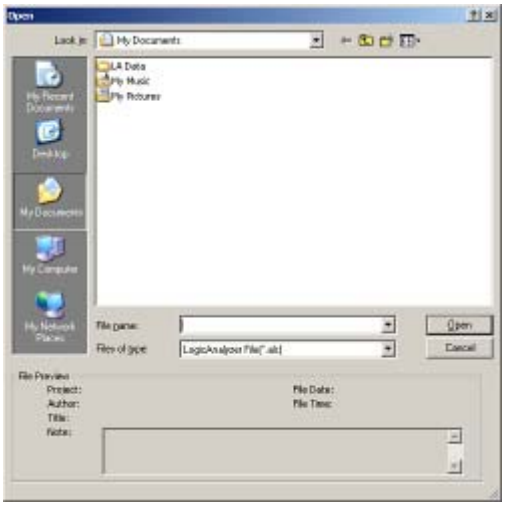
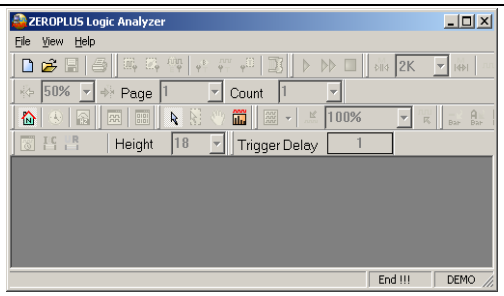
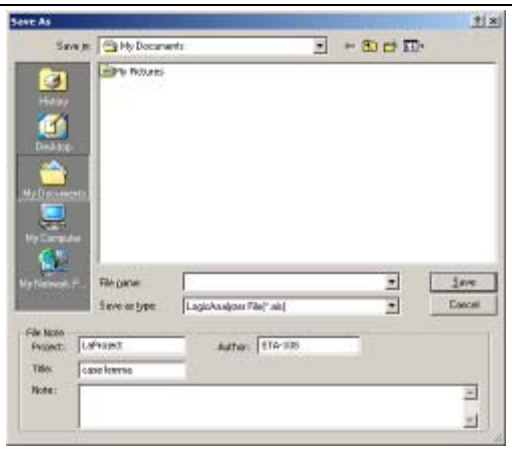


- **Close -** Close the file being worked on.
- **Auto Save -** Save the required file automatically (See **Section 3.4** for detailed instructions).
- **Export Waveform**- Export files into Text (*.txt) and CSV Files (*.csv)
- **Export Packet List**– Export the active packet list.
- **Language** - Allow users to change the language interface of menus, tool boxes, etc.
- **Print Preview** - Show three options: Bus/Signal & Bus & Filter columns, Waveform Display Area, and Position Display Area (See Fig. 3-14).
- **Exit** – Exit the program.

Fig 3-2: **File** Menu

Fig 3-3: **Standard** Tool Bar

Menu Bar: **File**

Menu Item	Detail Menu & Dialog Box
New Ctrl+N	Open a **New** file.
Open... Ctrl+O	 Fig 3-4: **Open** an existing file.
Close Ctrl+F4	 Fig 3-5: **Close** the active workspace.
Save Ctrl+S Save As... Auto Save	 Fig 3-6: **Save As** Window **Save –** Save the current file. **Save As –** Specify the name of the file to be saved. **Auto Save**- Save the required file automatically; users can decide the time.

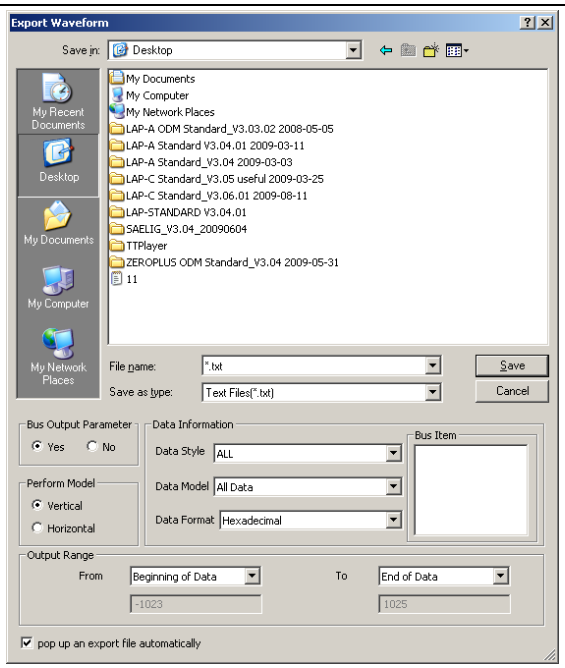


Fig 3-7: **Export Waveform** Window

Export Waveform: Export a file into text (*.txt) or CSV (*.csv) formats.

Bus Output Parameter: Decide whether or not to display the parameters of the file to be exported.

Perform Model: Choose whether to export the data either vertically or horizontally.

Output Range: Choose the range of the data to export from the pull-down menus.

Data Information:

Data Style: Include ALL, ALL BUS, PROTOCOL (HAS CHANNELS), PROTOCOL (NO CHANNELS).

Data Model: Export Data changed function; the selectable items include ALL Data, Sampling Changed Dot(Compression), Data Changed Dot (Compression). Some of the data value for the signal channels of sampling position are the same, for example, view the Data changed and decrease export capacity; this function will be good for users.

pop up an export file automatically:

The export file can be popped up automatically. Users can decide whether to activate the function; the default is selected. See the export file below:

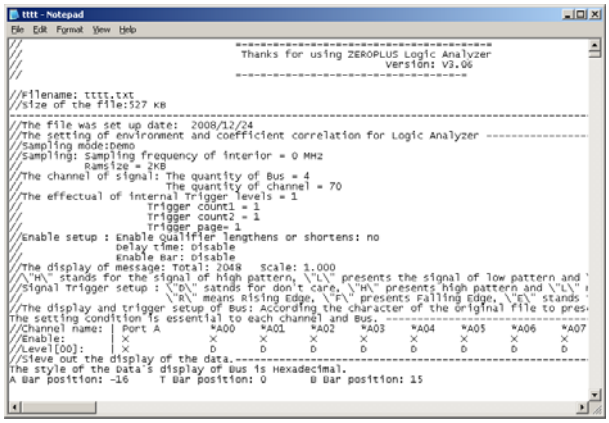


Fig3-8: Export File

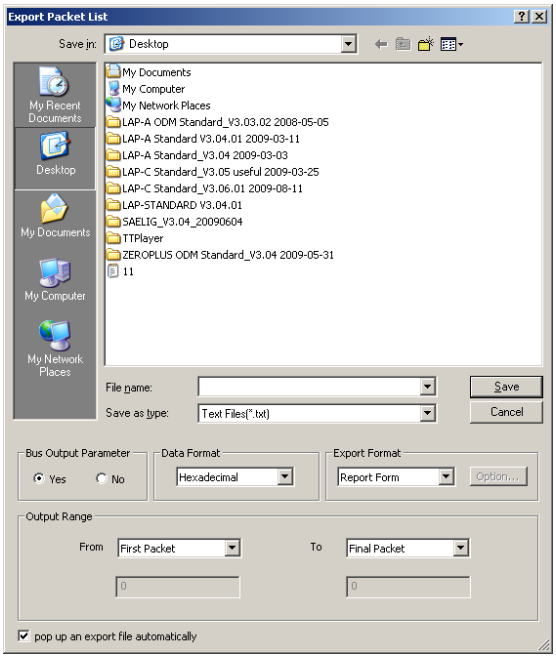


Fig 3-9: **Export Packet List** Window

Users can use paperwork, register and analyze packet list data.

The function of popping up an export file automatically in the Export Packet List dialog box is the same with that of the Export waveform for dialog box.

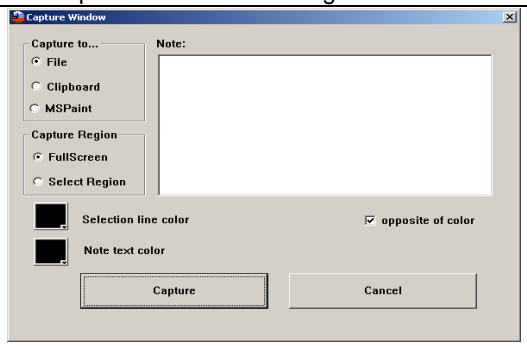


Fig 3-10: **Capture Window**

This feature is equivalent to [Alt]+[Print Screen], or [Print Screen]

Capture to

- File – Save the capture image as either a jpeg or a bmp.
- Clipboard – Copy the captured image to the clipboard for using in other applications.
- MSPaint – Directly start MSPaint to view the captured image.

Capture Region

- Full Screen – Capture everything on the screen.
- Select Region – After pressing the capture button, a cross-hair will appear on the screen. Left-click the mouse button to drag an area to capture.

Selection line color – Click the color box to change the color.

opposite of color – Click this check box to ensure that the note text will be the opposite of the line color.

Note text color – Choose the color of the note text.

Note – Type in a note to attach to the captured image.

Capture – Click the **Capture** button to capture the image.

Cancel - Click **Cancel** to end the capture.

Fig 3-11: Choose among Chinese Simplified (si), Chinese Traditional (Tr) and English.

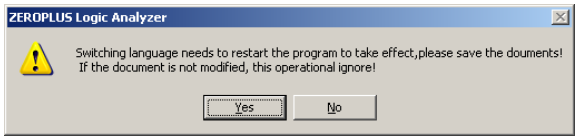


Fig 3-12: When changing languages, the above screen will be displayed and the program will need to be restarted.

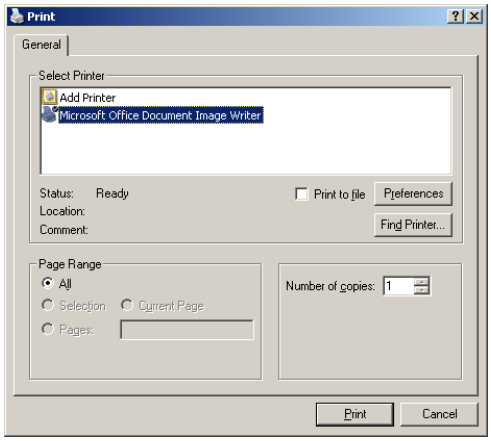
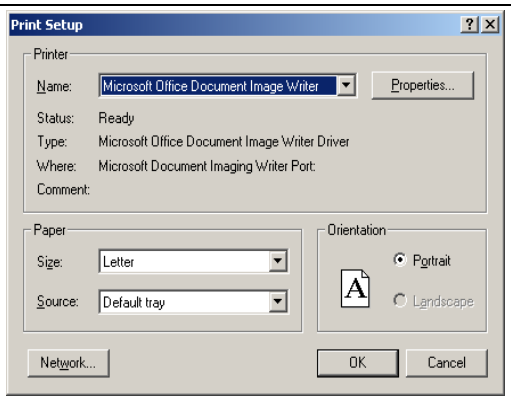


Fig 3-13: Click to enter the **Print** dialog box.

Fig 3-14: Click to show a **Preview** of the **Print**.

Print Setup...	 Fig 3-15: Click to enter the **Print Setup** dialog box.
Recent File	Show recently saved file.
Exit	Exit the program.

Bus/Signal

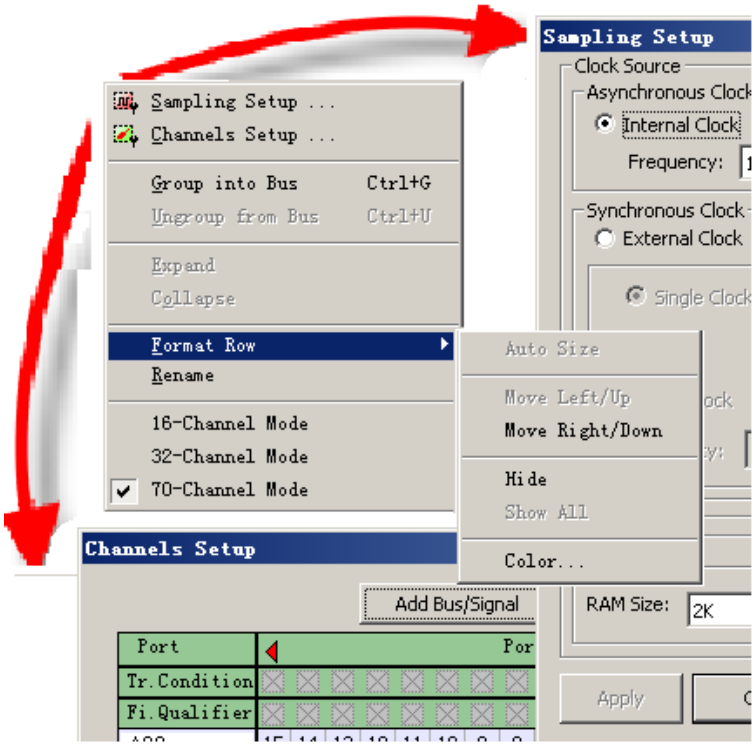


Fig 3-16: **Bus/Signal** Menu. Dialog boxes of the Sampling Setup and Channels Setup are shown and indicated by arrows.

Fig 3-17: **Trigger** Tool Box

Menu Bar: **Bus/Signal**

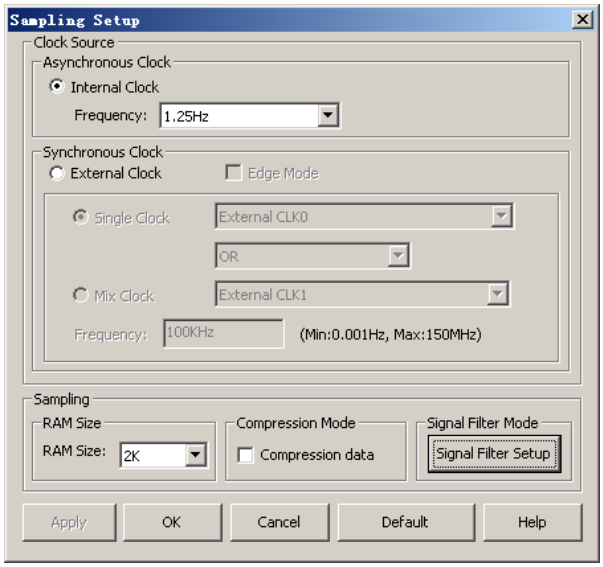
Menu Item	Detail Menu & Dialog Box
Sampling Setup ...	

Fig 3-18: Sampling Setup
See Section 4.1 for detailed instructions.

Tip:

Icon	Description
	Decrease RAM Size
	Increase RAM Size
	Decrease internal clock frequency
	Increase internal clock frequency

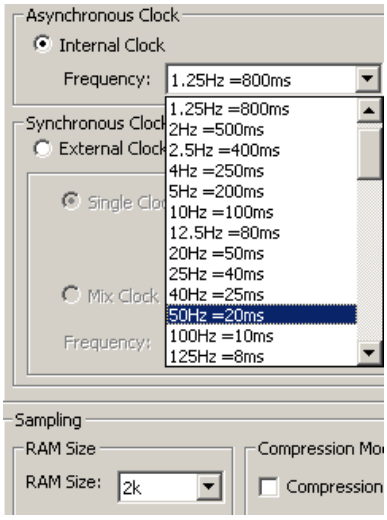
Fig3-19: RAM Size

Choose the RAM Size and the internal clock frequency from the pull-down menus.

RAM Size	The amount of acquired data that can be stored by the Logic Analyzer depends on the amount of allocated RAM Size. Take LAP-B (70256) as an example: The total depth of memory for the Logic Analyzer is 256K Bits in each probe. If the Logic Analyzer starts gathering data with a 128K memory range, it will take a long time to find the required information. In order to avoid spending a lot of time gathering data, select a smaller RAM Size. The RAM Size options are 2K, 16K, 32K, 64K, 128K and 256K.

Tip:

Clock Source
Asynchronous Clock

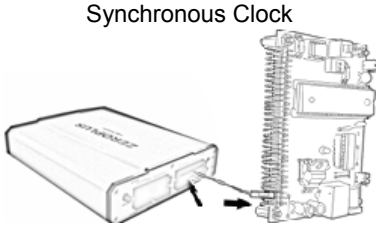


Sampling

Use the pull-down menu to choose the speed of the clock on the board being tested.

The sampling frequency should be more than 4 times higher than the signal to be measured so that the waveform duty cycle depiction will be accurate.

Synchronous Clock



Choose the frequency of the clock on the board of the Logic Analyzer. Select "External Clock" to acquire data through External sampling. Choose either "Rising Edge" or "Falling Edge" to execute the analysis process.
According to the users input the value of external frequency in software, the software can count the relevant value about signal mode and frequency. For example: the value of the message, the time scale and the zoom in and out will be the value of time mode.

Connecting the Synchronous Clock:
Use one of the single connecting cables, put one end on the mother board and the other in the LA as shown in the diagram opposite.

Tip:

Compression

Check the box to compress all the data.
Compression is used for compressing the acquired data through a lossless compressor. The purpose of this compression is to place more data in limited memory than in actual memory. The compression rate of the Logic Analyzer can be up to 255 times. Taking the memory being 128K as an example, this means that the maximum acquisition can be 32M Bits (128Kx255= 32M Bits) for each channel. The chosen capacity of the memory, 1MB, means that the maximum data being sieved out arrives at 1MB*255=255M Bits (Per Channel).
Note: The rate will change depending on the data being analyzed.

Tip:

Signal Filter Setup

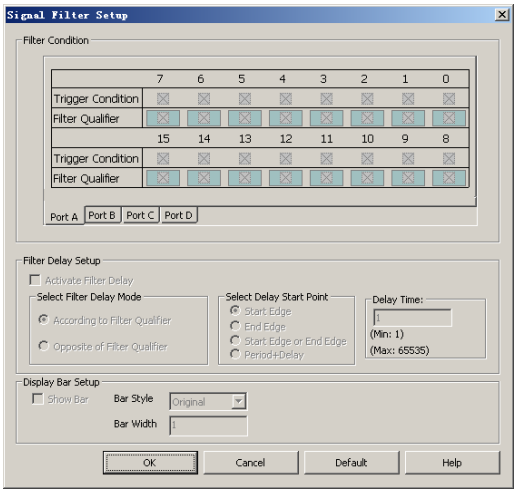


Fig 3-20: Dialog Box: **Signal Filter Setup**

Tip:

Click to enter the Signal Filter Setup screen.

The function of Signal Filter is to use an alterable judgment circuit which can filter undesired signals in order to capture and store valuable data in the memory. When the combination of input signals from each channel is satisfied with the conditions of "Signal Filter Mode", the section of acquired data will be gathered by the Logic Analyzer and stored in the memory. After storing the data, it will return to the Logic Analyzer's system and be displayed as a waveform. If the combination is not satisfied with the conditions of "Signal Filter Mode", the Logic Analyzer won't gather and store data.

Tip:

There are 3 modes of Signal Filter configuration for each channel.

1. = Don't Care means that the Logic Analyzer captures all signals from sampling.

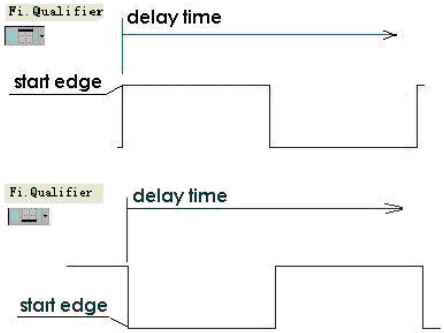


Fig 3-21: High and Low Levels

It is the system default.

2. = High Level means that the Logic Analyzer captures and displays the input signals satisfying the high level.

3. = Low Level means that the Logic Analyzer captures and displays the input signals satisfying the low level.

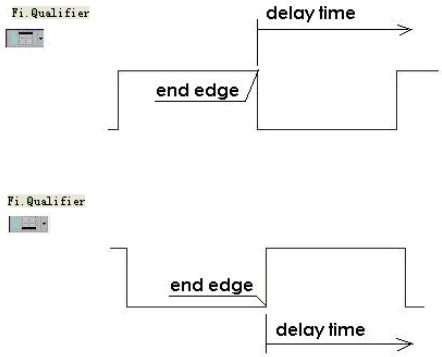


Fig 3-22: High and Low Levels
Filter Delay Setup

Filter Delay – According to Filter Qualifier.
Start Edge – Show the waveform start edge to delay time interval.

See details in Section 4.1 Tasks 1 and 2.

Tip:

Channels Setup

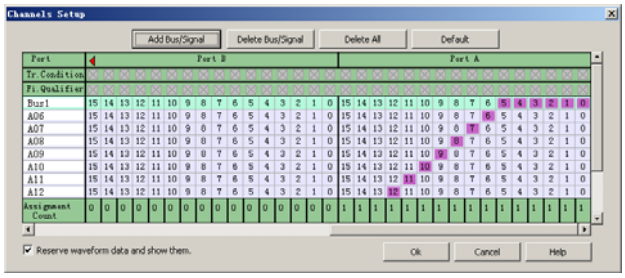


Fig 3-23: **Channels Setup**

See details in Section 4.2.

Tip:

Add Bus/Signal	Click the **Add Bus/Signal** button to add a port. This will appear as 'New'. Click the port(s) to be added to the new signal.
Delete Bus/Signal	Click the Bus you want to delete and then press the **Delete Bus/Signal** button.
Delete All	Press the **Delete All** button to delete all the Buses.
Default	Press **Default** to return all channels and Buses to the system defaults.
Reserve waveform data and show them	Select this function when having added or deleted channels, the software reserves the original waveform; not select this function, the waveforms in channels are cleaned up.

Group into Bus Ctrl+G	Signals can be grouped into Buses by pressing **Ctrl + G**. Signals can be added, deleted ,copied and grouped into Bus. Use the mouse or the keyboard, or right click and select Properties from the popup dialog box, the functional form of sampling setting. The untied Data Bus is a signal line; the signal line means Data Bus. The movement of a signal line, from up to down, are **Auto Size**(not available in waveform display), **Move Up**, **Move Down**, **Hide, Show All** and **Color**).
Ungroup from Bus Ctrl+U	**Ungroup** signals **from Bus** by pressing **Ctrl + U**.

Expand

A Bus contains at least 1 signal channel. In order to see these signals click the '+' symbol before the name of the Bus.

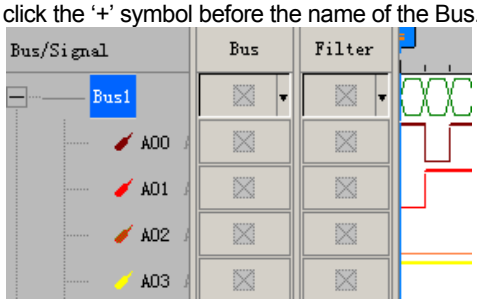


Fig 3-24: Expand

Collapse

If the Bus has been expanded, click the '-'symbol before the Bus name to **Collapse** the Bus.

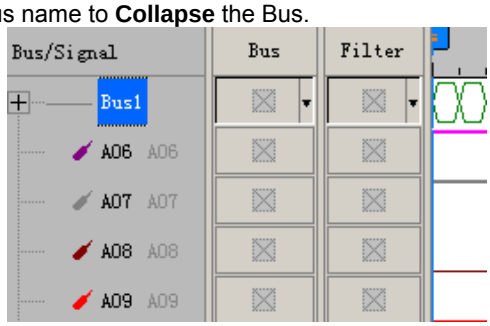


Fig 3-25: Collapse

Format Row

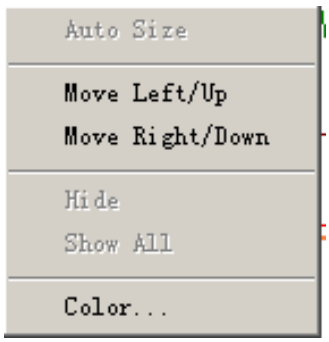


Fig 3-26: Click to change the Bus or signal display

Tip:

Format Row	Change the display of a Bus or a signal.
Auto Size (NOT Available in waveform Display)	Size the signal columns automatically.
Move Left/Up (Change to Move Left in Listing Display)	Highlight a signal or Bus and click **Move Left/Up** to move the signal or Bus up (left) through the list of the Bus/Signal.
Move Right/Down (Change to Move Right in Listing Display)	Highlight a signal or Bus and click **Move Right/Down** to move the signal or Bus down (right) through the list of the Bus/Signal.
Hide	Highlight a signal or Bus and click **Hide** to hide it.
Show All	Click **Show All** to show all signals and Buses that have been hidden.
Color	Highlight a signal or Bus and click **Color** to change the color.

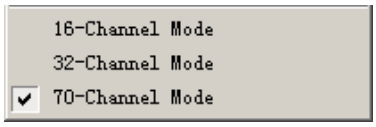
Rename

Tip:

When users select one channel to change the name of the channel, users can rename other channels

Highlight a signal or Bus and click **Rename** to rename the Bus or signal.

fast by clicking the up and down arrows on the keyboard.



Channel Mode（only for LAP-B(702000+)）:
There are three modes for **LAP-B(702000+)**, which are 16-Channel Mode, 32-Channel Mode and 70-Channel Mode; the default is 70- Channel Mode.

16-Channel Mode: There are only 16 channels available; the max. RAM Size is 8M and the max. Sampling Frequency is 1000MHz.

32-Channel Mode: There are only 32 channels available; the max. RAM Size is 4M and the max. Sampling Frequency is 500MHz.

70- Channel Mode: Keep the parameter of the P-B(702000). There are 70 channels available; the max. M Size is 2M andthe max. Sampling Frequency is 333MHz.

Tip:

The purpose of adding the 16-Channel Mode and 32-Channel Mode is to improve the Sampling Frequency. The typical Sampling Frequency is above 400MHz which is over the input bandwidth of the External Clock, so, in the 16-Channel Mode and 32-Channel Mode, when the functions of Signal Filter and Compression are closed, the function of the External Clock is also to be closed.

Trigger

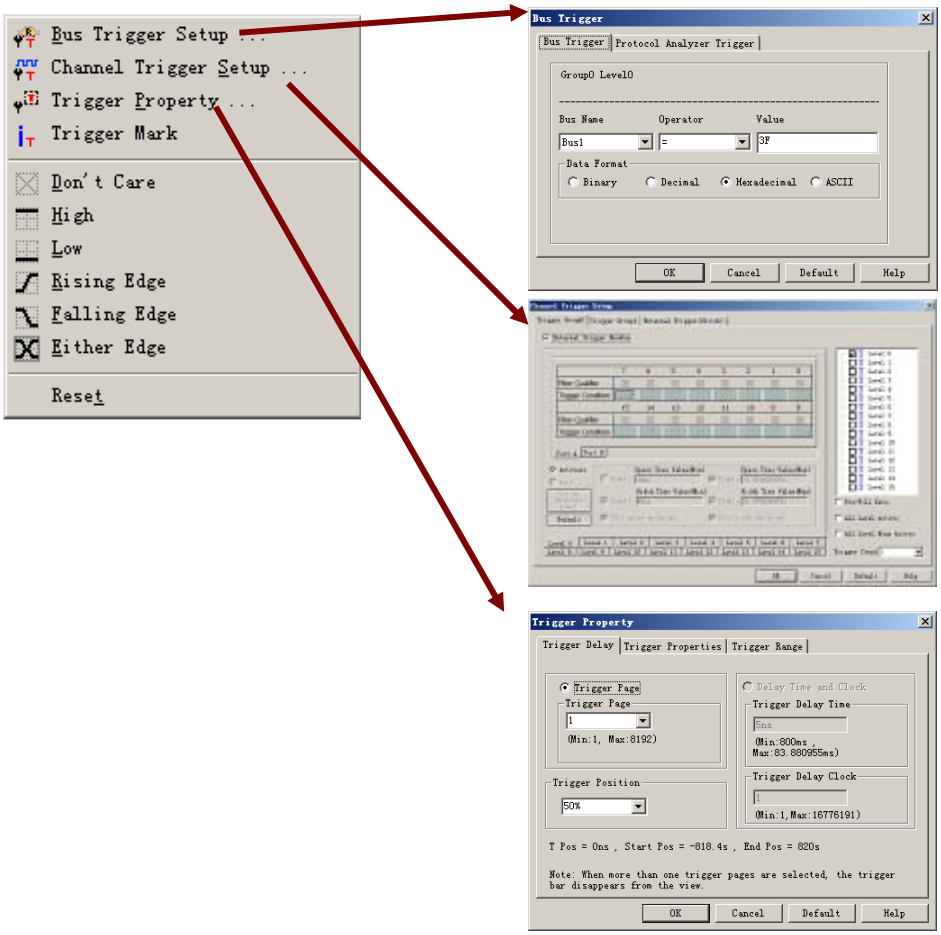
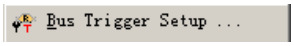
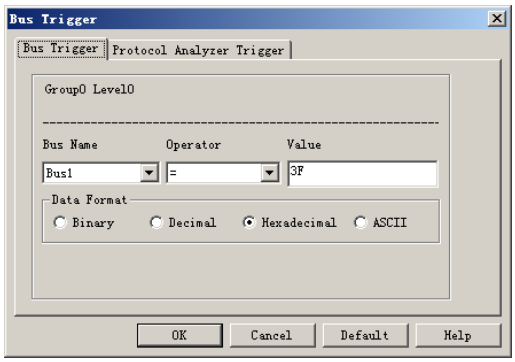
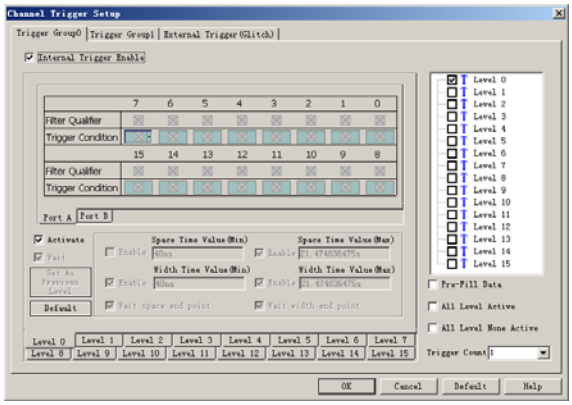
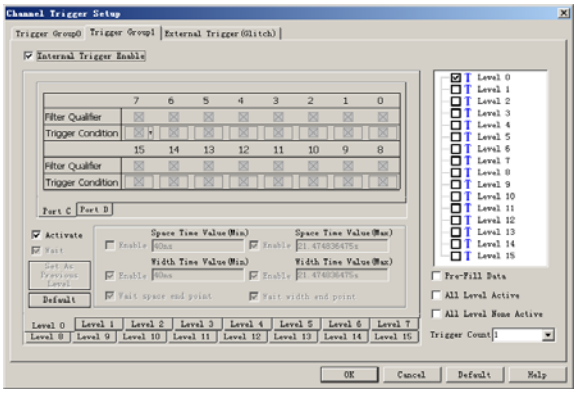


Fig 3-27: **Trigger** Menu

Fig 3-28: **Trigger** Tool Box

Menu Bar: **Trigger**

Menu Item	Detail Menu & Dialog Box
	 Fig 3-29: Set **Bus Trigger**. See Section 4.1 and 4.2 for detailed instructions.
 Tip: The trigger action tells the Logic Analyzer when to send data to the PC. The trigger conditions determine when the trigger point starts to record the information.	 Fig 3-30: Set **Trigger Group0**.  Fig 3-31: Set **Trigger Group1**. Fig 3-32: Set **Trigger Count**. See Section 4.1 for detailed instructions.

Tips:

External Trigger (Glitch):
Enable External Trigger (Glitch): Activate the first group external trigger. It includes four selections which are EXT Trigger0, EXT Trigger 1, EXT Trigger 2 and ~ EXT Trigger0.
Enable Two Trigger In: Activate the second group external trigger. It includes four selections which are EXT Trigger0, EXT Trigger 1, EXT Trigger 2 and ~ EXT Trigger1. When you start it , you can start the logic operation with the first one group.
Trigger Out Enable: Set the output trigger condition.
There is an output point for the hardware, and it can be selected by the software (three selections are **When Trigger Condition**, **START** and **STOP**).
From LAP-B Trigger Out Sync: It can accept the trigger signal from another Logic Analyzer.

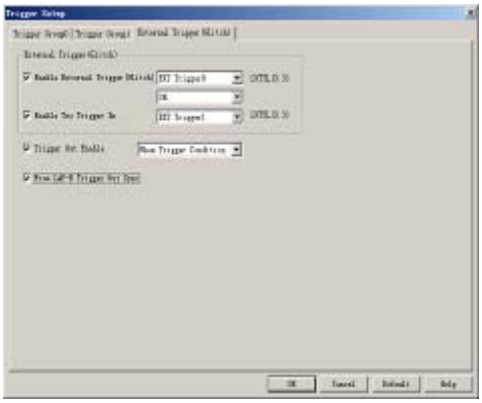
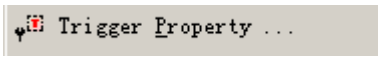


Fig 3-33: Set **External Trigger**.



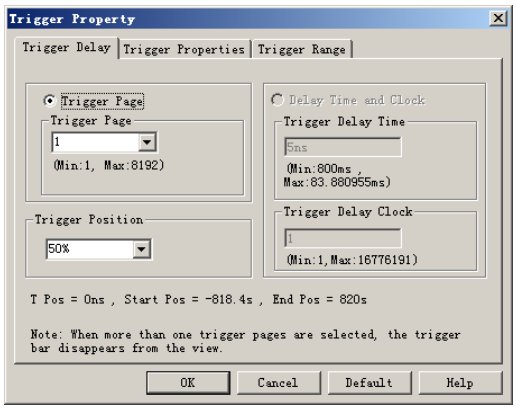


Fig 3-34: Set **Trigger Delay**.

Tips:
The voltage level that a trigger source signal must be reached before the trigger circuit initiates a sweep.
There are 4 ports available; Each port has the ability to assign different voltages to meet the users' requirements.
Use the pull-down menu to choose between TTL (default TTL), CMOS (5V), CMOS(3.3), ECL and User Define (choose the value of the Trigger Voltage between – 6.0V and 6.0V).

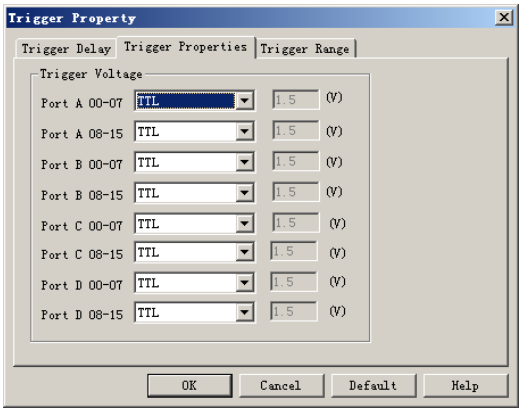


Fig 3-35: Set **Trigger Properties**.

Tips:
When the Bus data is too long, the default trigger mark bar can't meet the need of the mark of the current Bus single function, so we add the function of Trigger Mark Setting. Users can set the number of the trigger mark bar as their requirements, and then more bars which conform to the current trigger data to be marked.

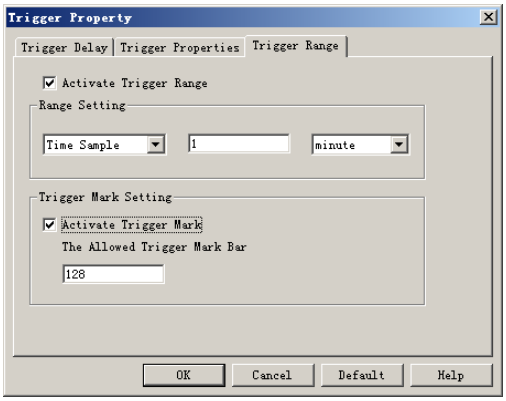


Fig.3-36: Set **Trigger Range**.
See Section 4.1 for detailed instructions.

Trigger Mark	Trigger Mark Fig3-37: Click to open the Trigger Mark function. See Sections 4.1 for detailed instructions.
Don't Care	Set the trigger condition as "**Don't Care**" See Section 4.1 for detailed instructions.
High	Set the trigger condition as "**High**" See Section 4.1 for detailed instructions.
Low	Set the trigger condition as "**Low**" See Section 4.1 for detailed instructions.
Rising Edge	Set the trigger condition as "**Rising Edge**" See Section 4.1 for detailed instructions.
Falling Edge	Set the trigger condition as "**Falling Edge**" See Section 4.1 for detailed instructions.
Either Edge	Set the trigger condition as "**Either Edge**" See Section 4.1 for detailed instructions.
Reset	Reset the trigger condition.

Run/Stop

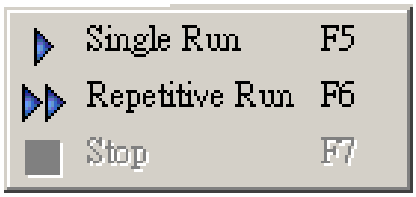


Fig 3-38: **Run/Stop** Menu

Fig 3-39: **Run/Stop** Tool Box

Menu Bar: **Run/Stop**

Menu Item	Detail Menu & Dialog Box
Single Run F5	Click to run once. See Section 4.1 for detailed instructions.
Repetitive Run F6	Click to run continuously until the **Stop** button is pressed. See Section 4.1 for detailed instructions.
Stop F7	Click to stop the repetitive run. See Section 4.1 for detailed instructions.

Data

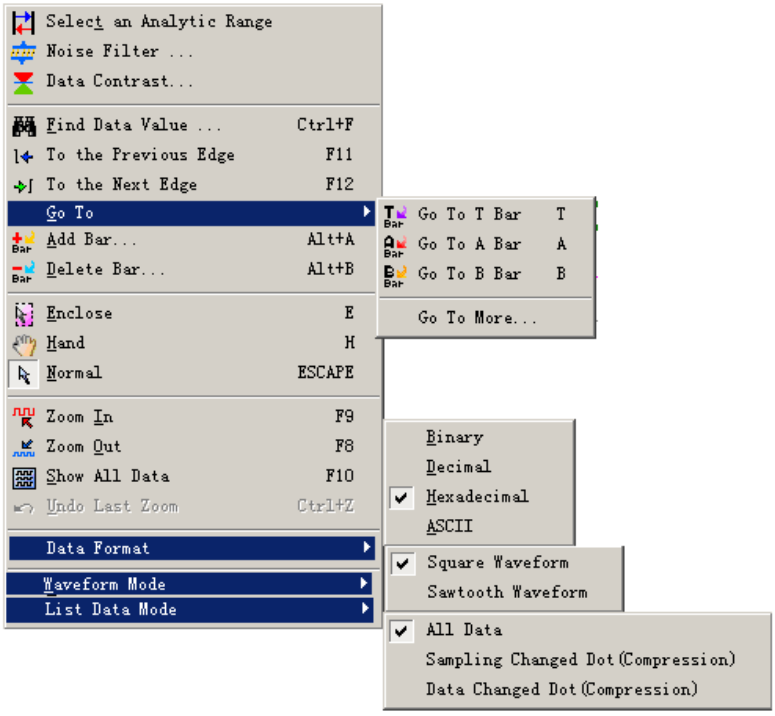
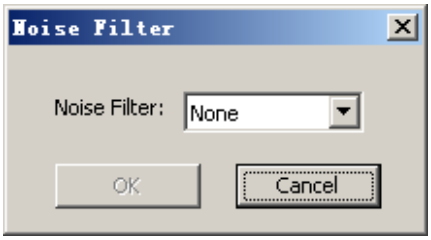
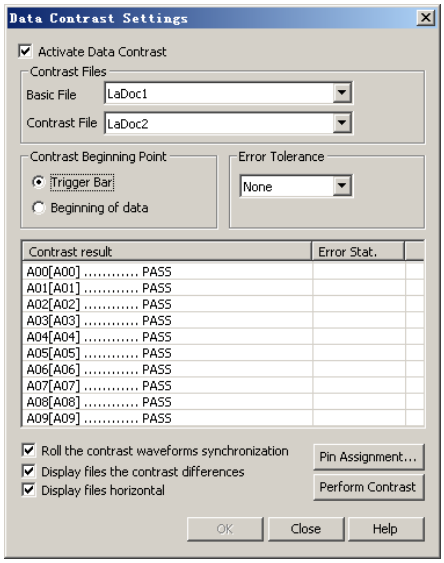
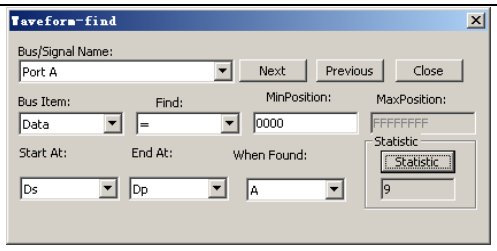


Fig 3-40: **Data** Menu

Fig 3-41: **Data** Tool Box

Menu Bar: **Data**

Menu Item	Detail Menu & Dialog Box
Select an Analytic Range	Check the box to make the analytic range changed by dragging the Ds and Dp holders with the left mouse button.
Noise Filter ...	Noise Filter: It can filter 0~10 Clock Width's positive pulse or negative pulse signal.  Fig3-42: Noise Filter See Section 4.9 for detailed instructions.
Data Contrast...	 Fig3-43: Data Contrast Settings Contrast the difference of data. It is used for contrasting the difference between two signal files of the same style. One is the Basic File, the other is the Contrast File, which can display the difference from the Basic File.
Find Data Value ... Ctrl+F	 Fig 3-44: Waveform-find Setup
Tip:	Use the pull-down menu to select the Bus / Signal

Remember the last setting: When the Find function is activated, it will display the last setting. When you have closed the Waveform-find dialog box,and you want to know the last setting, you can open the Waveform-find dialog box again for the system has saved the last setting conditions automatically.	Name: The list of characters depends on whether it is a Bus or Signal that is being searched in: **Bus** – Choose among =, !=, In Range and Not In Range (enter the value for MinPosition and MaxPosition). **Signal** – Choose among Rising Edge, Falling Edge, Either Edge, High and Low. **Start At** – Ds, T, A, B(select from the pull-down menu). **When Found** – Dp, A, B(select from the pull-down menu). **Statistic** – Show the number of the search results. **Note:** It is available only when searching through a Bus.
To the Previous Edge F11	Go to the previous edge sweep of the indicated signal.
To the Next Edge F12	Go to the next edge sweep of the indicated signal.

GoTo ▸

Go To T, A, B, or **Go To** More.

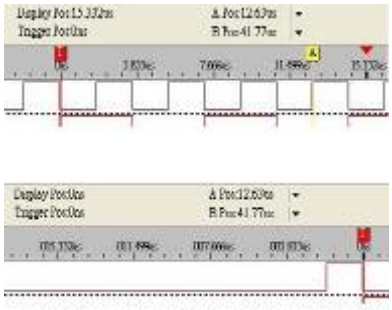
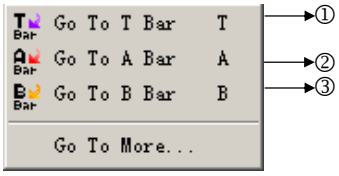


Fig 3-45: T Bar will be displayed in the center of the waveform area.

Tip:



① Press T, go to T bar.
② Press A, go to A bar.
③ Press B, go to B bar.

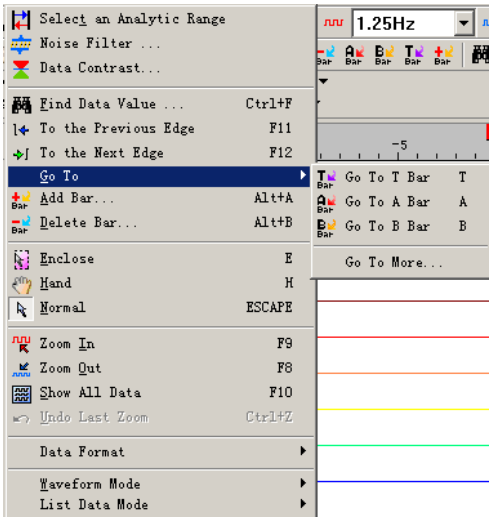


Fig 3-46: The selected bar will be shifted to the center of the waveform area.

Add Bar... Alt+A

Add user defined bars.

1. Click the above menu item from **Data** menu, or click **Add Bar** icon from the tool box.
2. Give a **Bar Name**, define a **Bar Color**, and enter a **Bar Pos**ition.
3. Define the **Bar Key** with the number between 0 and 9.

Tip:
The number shortcut key is set in the **Add Bar** dialog box. Every new bar can be filled in one number, which is used to find the required bar faster; the default number of the new bar is 0. It is noticed that once the number key is set, it can't be modified; and each new bar can be named with the same number, that is to say, one number can name many bars.

For example, users can set the number 3 as the shortcut key. When users press the number 3 key, the C Bar will be displayed in the centre position of the screen .

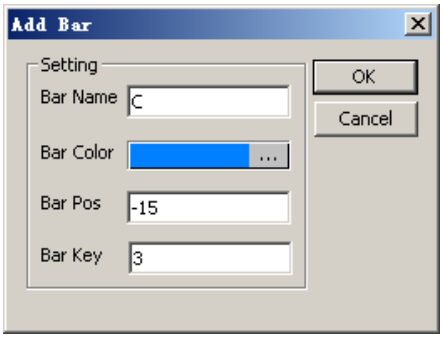


Fig3-47: Add Bar

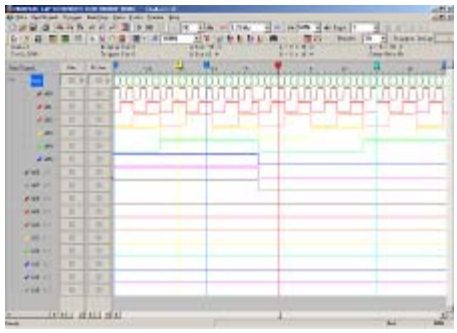


Fig3-48: Add Bar with the number between 0 and 9.

Delete Bar... Alt+B

Delete a defined bar by users.

1. Click the above menu item from **Data** menu, or click **Delete Bar** icon from the tool box.
2. Select a defined bar by users, and click **Delete**.
3. Delete the selected bar with the **Delete Key** on the **Keyboard.** Use the mouse to select the added bar and press the **Delete** key on the keyboard to delete the bar.

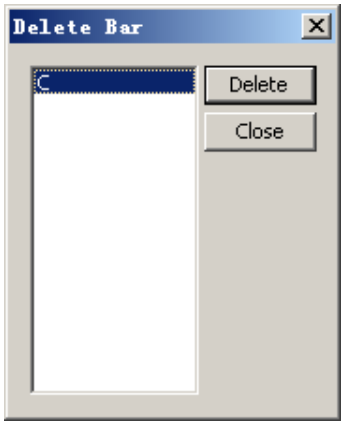


Fig3-49: Delete Bar Dialog Box

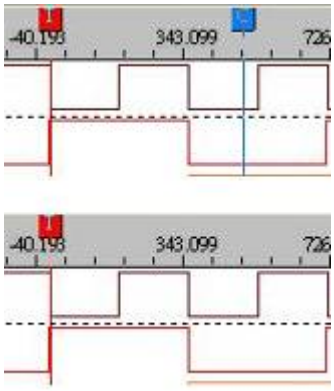


Fig 3-50: Delete a selected Bar.

Enclose E

1. A Zoom-In or a Zoom-Out view will be centered in the Position of Display Area, and the new zoomed view will be sized according to the available space on the display.

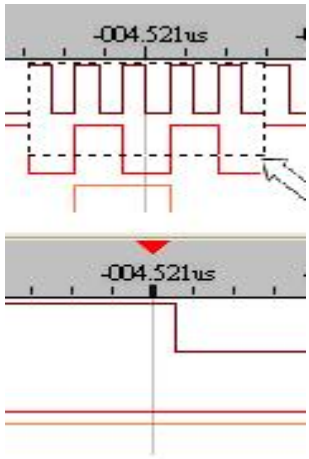


Fig 3-51: To **Zoom In**, left click and drag the mouse pointer from left to right.

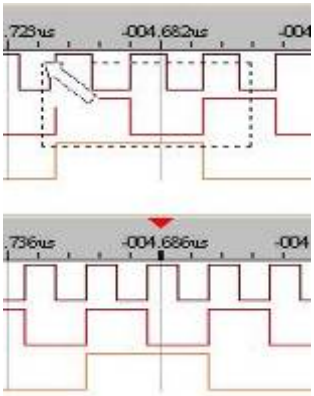


Fig 3-52: To **Zoom Out**, left click and drag the mouse pointer from right to left.

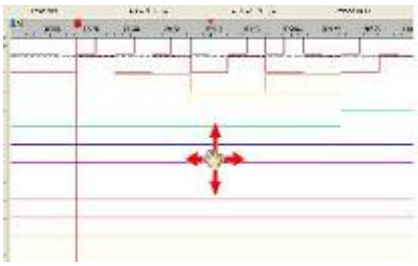
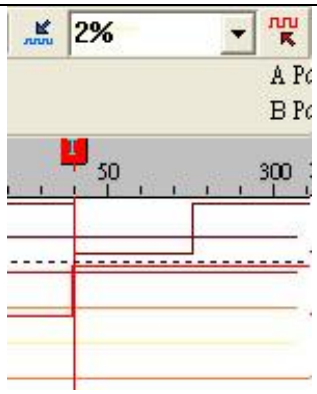
2. When users activate the Enclose to zoom in / zoom out the selected area, the Tooltip on the right corner of the bottom will display the Time, Frequency or Address of the selected area.
When selecting the Enclose function, and users are pressing and dragging the left key, the information on the right corner of the bottom will be changed and updated with the width of the selected area. And the information is displayed on the right corner of the bottom in the way of Tooltip. When users loosen the mouse, the information will disappear.

Fig 3-53: To display the Tooltip, left click and drag the mouse pointer from right to left or from left to right.

Tooltip:

Time/Frequency Mode: Time/ns

Address Mode: Address

Hand H	 Fig 3-54: Click Hand, and then press and hold the left mouse button to drag.
Normal ESCAPE	Reset the mouse pointer function.
Zoom In F9 Zoom Out F8	 Fig 3-55: Normal status

Tips:

Zoom In and Out can be switched by changing the percentage value in the pull-down menu.

1. The system can set the value of Zoom In and Out:

   The default unit is μs, when zooming in, it will be automatically changed to ns; when zooming out, it will be changed to ms, s or ks.

2. Pull-down menu:

   There are thirty scales.

   The maximum zoom in and out is the cycle of each grid, 0.0001piece.

   The minimum zoom in and out is the cycle of each grid, 1,000,000,000.

   Zoom In and Out (the proportion): with each grid being the cycle, the zoom in and out (%) is 100%. The time of zoom in and out counts by the clock of each grid (sample frequency). For example:

   (1) Each grid is being a cycle; the zoom in and out is 100%. The time of zooming in and out will be presented by the clock of each grid X (1/sample frequency).

   (2) Each grid stands for the clock of 100 pieces; the zoom in and out is 1% and the time of zooming in and out will be displayed by the cycle of each grid X (1/sample frequency).

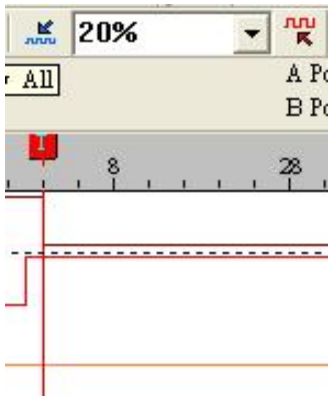


Fig 3-56: Result from normal to **Zoom In**

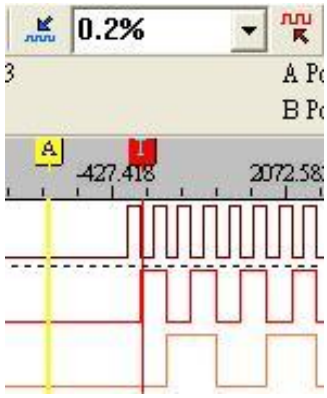


Fig 3-57: Result from normal to **Zoom Out**

Fig 3-58: **Show all Data** of a memory page

Return to the last zoom.

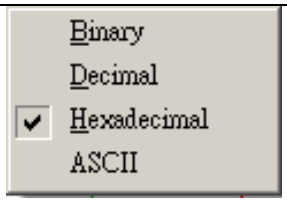


Fig3-59: Data Format

Show numerical information in binary, decimal, hexadecimal, or ASCII format.

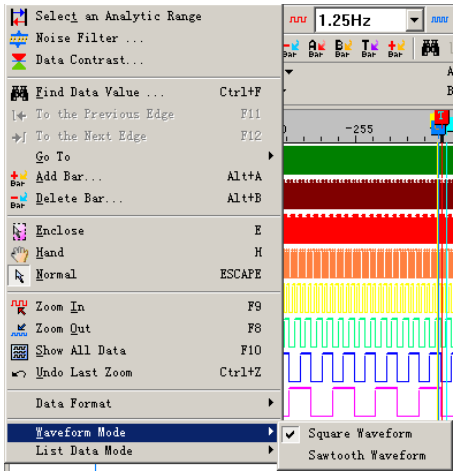
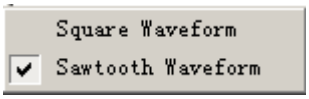


Fig 3-60: **Waveform Mode** in the Square Waveform.



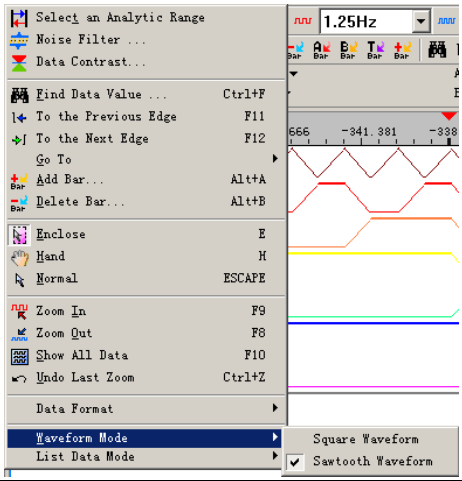


Fig 3-61: **Waveform Mode** in the Sawtooth Waveform.

Tip:

The data of Listing Display Mode are so many, to be convenient for users, that it adds the function of displaying data changed dot.

The format for the data display:

All Data, Sampling Changed Dot(Compression), Data Changed Dot(Compression).

All Data: It is the present display mode.

Sampling Changed Dot (Compression): Take the sampling changed dot as the compression data reference dot.

Data Changed Dot (Compression): Take the present data change dot as the compression data reference dot .

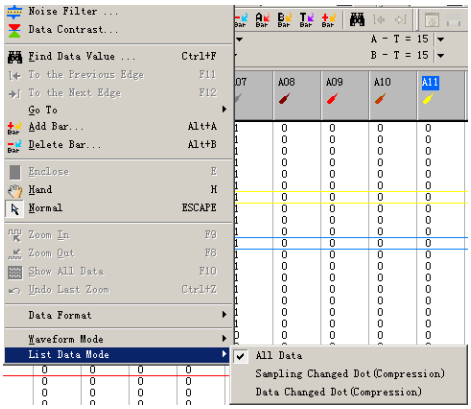


Fig 3-62: Show the List Data Mode: All Data, Sampling Changed Dot(Compression), Data Changed Dot(Compression).

Tools

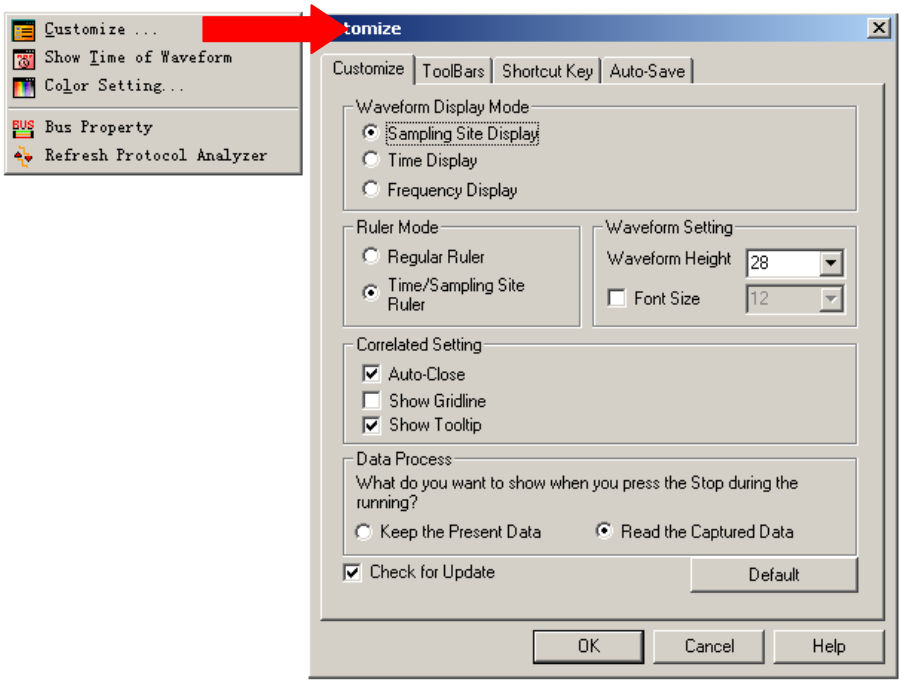


Fig 3-63: **Tools** Menu

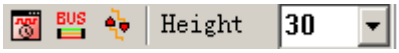
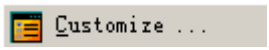
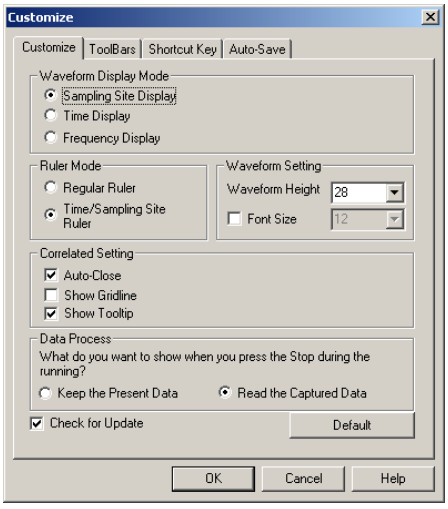
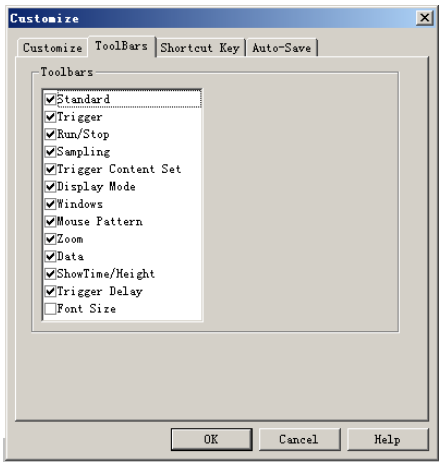


Fig 3-64: **Mouse Pattern** Tool Box

Menu Bar: **Tools**

Menu Item	Detail Menu & Dialog Box
	
See Section 3.4 for detailed instructions.	Fig 3-65: **Customize** the workspace. **Waveform Height:** The setup of the waveform swing height. It also can be set in the toolbox menu. **Font Size:** The character data of the waveform field. User can customize the Font Size, but it is not convenient for operating.The range of Font Size is from 1° to 180° . On condition that it is the default, the Font Size hides the change of Waveform Height.  Fig 3-66: Customize **ToolBars**

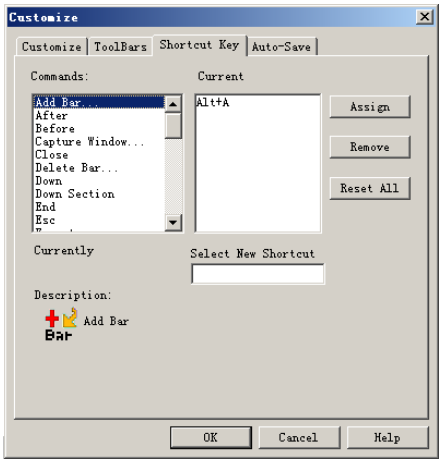


Fig 3-67: Customize **Shortcut Key**

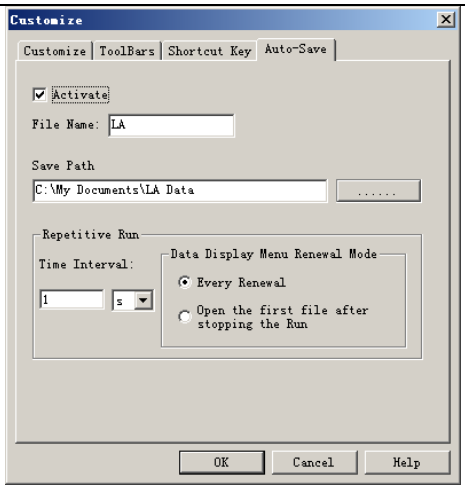
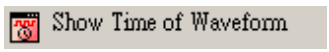


Fig 3-68：Customize **Auto-Save**

See Section 3.4 for detailed instructions



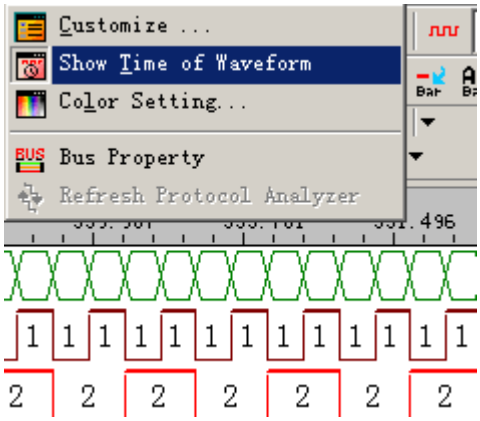


Fig 3-69: **Show Time of Waveform** under Sampling Site Display Mode.

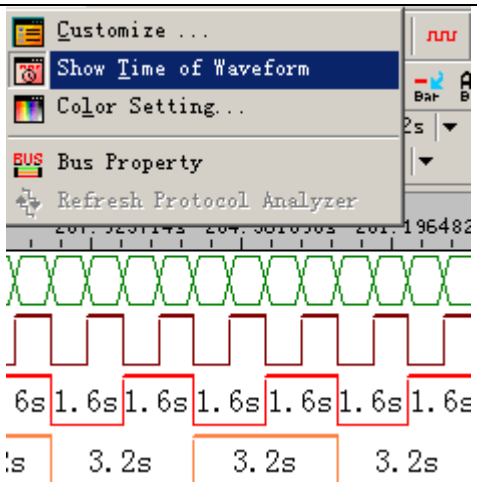
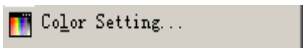


Fig 3-70: **Show Time of Waveform** under Time Display Mode.



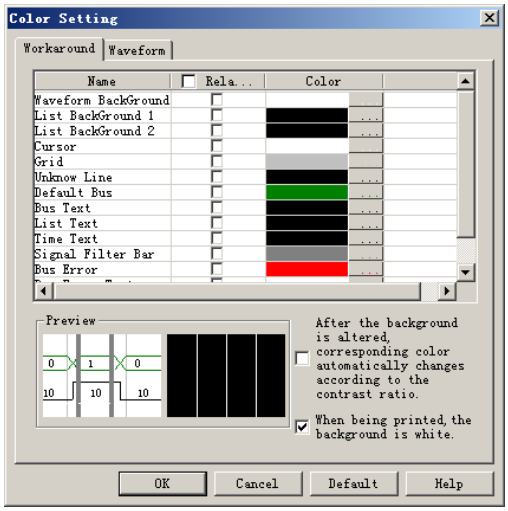
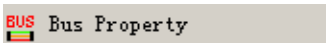


Fig 3-71: **Color Setting**.
See Section 3.5 for detailed instructions.



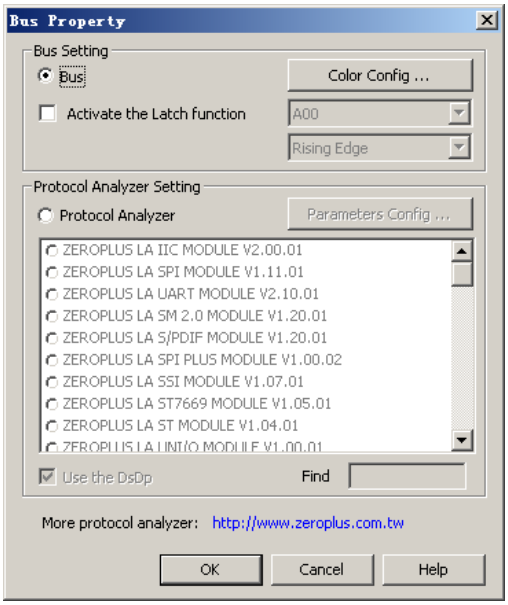


Fig 3-72: **Bus Property**

Bus: Activate the function of analyzing the Bus.

Color Configuration: Open the Color Configuration dialog box to set the conditions for the Bus.

Activate the Latch function: Activate the latch function.

Protocol Analyzer: Activate the function of analyzing the Protocol Analyzer.

Use the DsDp: Use the Ds and Dp to help analyze the Protocol Analyzer.

Find: Find the desired Protocol Analyzer module. Users can input the Protocol Analyzer name to quickly find the Protocol Analyzer module from many Protocol Analyzers. After inputting the first character of the name in the Find box of Bus Property dialog box, the corresponding module will be displayed in the Protocol Analyzer list box according to the input character. See the figure below:

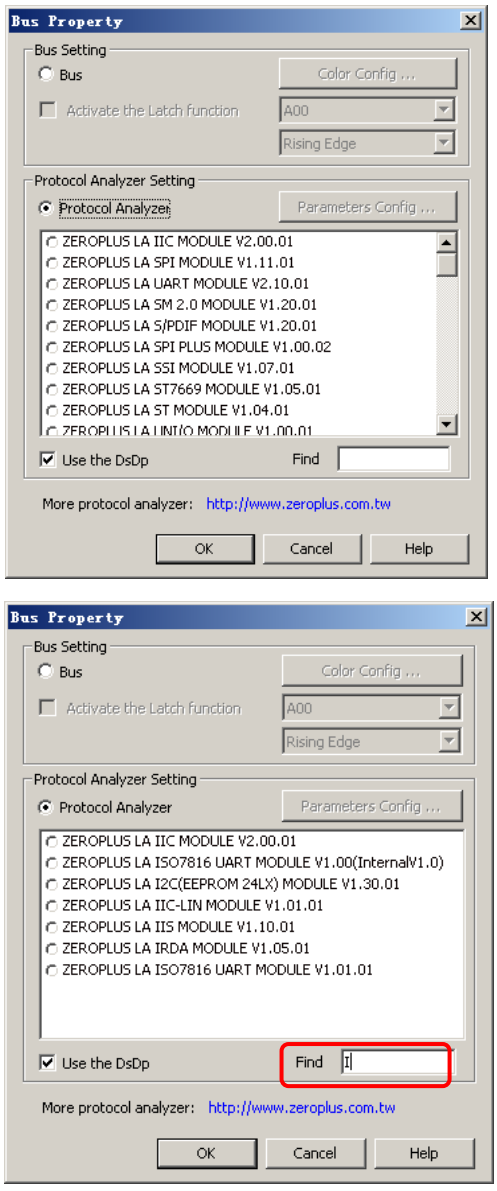


Fig 3-73: Activate **Find** function

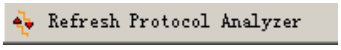


Fig 3-74: **Refresh Protocol Analyzer**

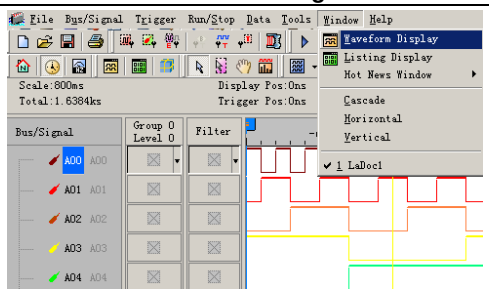
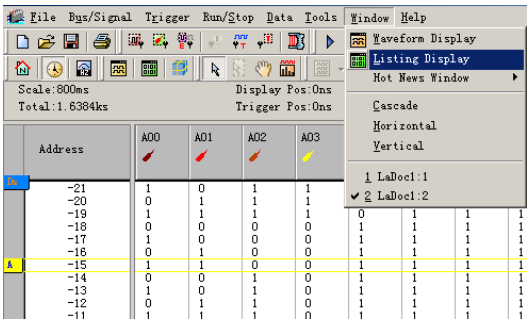
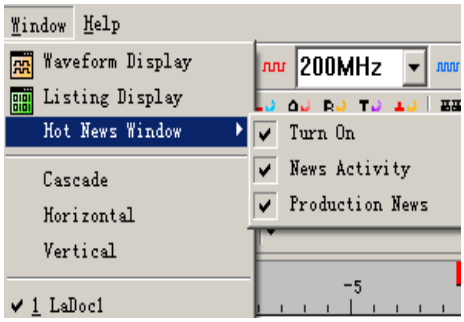
See Section 4.10 for detailed instructions.

Window

Fig 3-75: **Window** Menu

Fig 3-76: **Window** Tool Box

Menu Bar: **Window**

Menu Item	Detail Menu & Dialog Box
Waveform Display	
	Fig 3-77: **Display** signals in **Waveform Mode**.
Listing Display	
	Fig 3-78: **Display** signals in **Listing Mode**.
Hot News Window	
	Fig3-79: Running–Text Ads Function
Tips: Running-Text Ads Frame renews	**Tip:** To let online users learn the latest news, we add the Running–Text Ads Function. **Turn On**：Start the Running-Text Ads function. **News Activity:** Let users learn the activities of our company. **Production News:** Let users learn the latest products of our company. **Note**：It includes updating the software and Protocol Analyzer module or issuing the new mechanism, to make the online users know the newest information about our

every 0.5s and adds a character, and the displayed content moves from right to left. When one item's character displays completely, it will rest 3s, and then displays the following characters. When removing the cursor to the frame, the character will stop moving; when withdrawing the cursor, the character will go on moving.

If both News Activity and Production News are turned on, the Running-Text Ads will play News Activity prior to Production News and play the news in order. The whole process plays repetitively.

company according to the mechanism style of the net list.

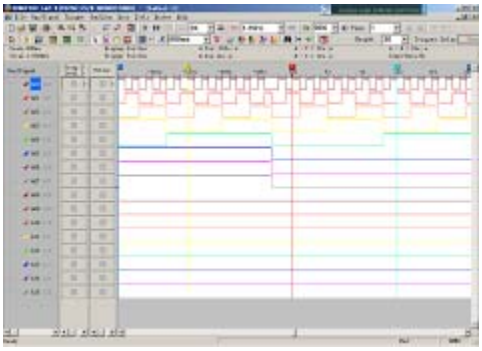
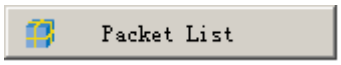


Fig3-80: Display **Hot News Window** in the window interface

Fig 3-81: Image Interface



Tip:

Setting: Run Packet List to set up the content of the packet.

Refresh: Click it, and then the content in the Packet List will be refreshed.

Export: Users can use a fragment to work, record and analyze the Packet List data.

As Export, according to the Packet List arrangement, it will export the txt. file and csv. file.

Synch Parameter: Open the packet and waveform synchronization setting dialog box.

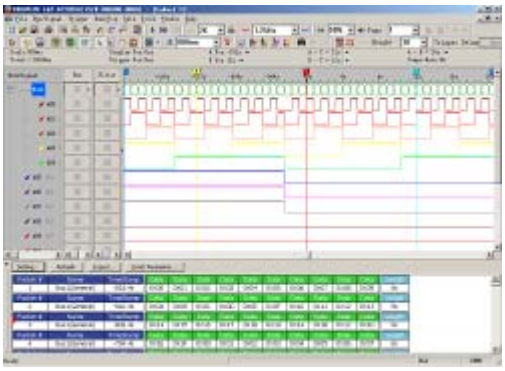


Fig3-82: Display Packet Content in Packet List.

Cascade

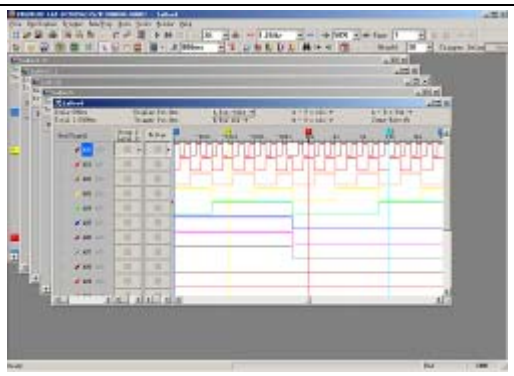


Fig 3-83: **Cascade** Workspace(s)

Horizontal

Fig 3-84: Align workspace(s) **Horizontal**ly.

Vertical

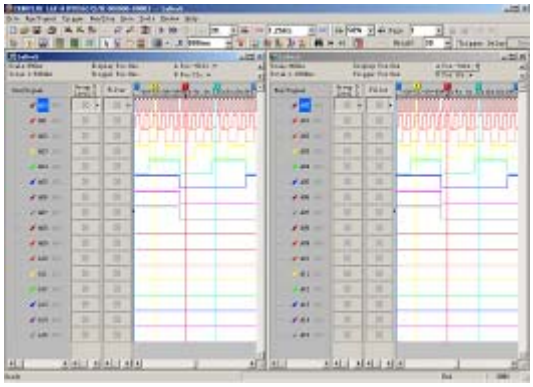


Fig 3-85: Align workspace(s) **Vertical**ly.

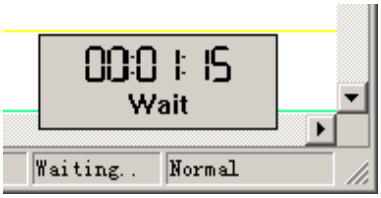


Fig3-86: Stopwatch Function

Stopwatch Function:

The function will show at the right corner of the bottom of the screen while sampling data. It times from users pressing the ensured key at the Bus Property dialog box to Bus insert sending back the analyzed data. It has five functions as following: Time of waiting for triggering, Time of triggering success, Time of sampling data, Time transmitted to computer after sampling data finished, Time of Bus data overloading.

Help

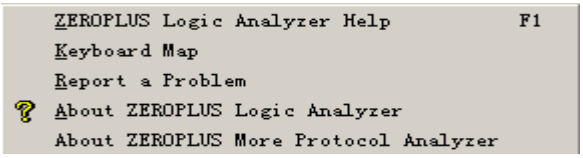
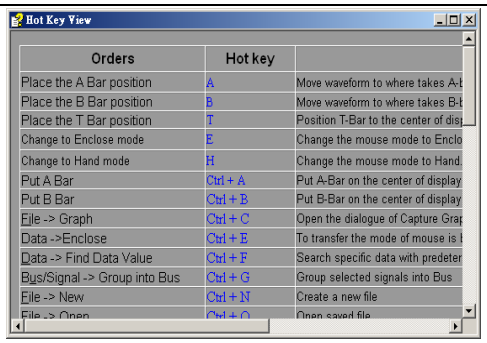
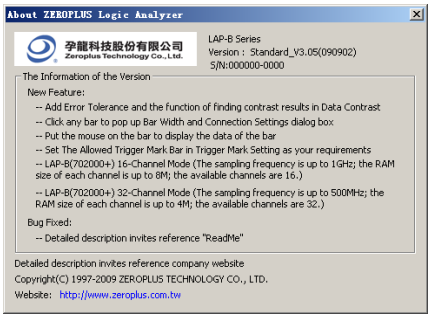


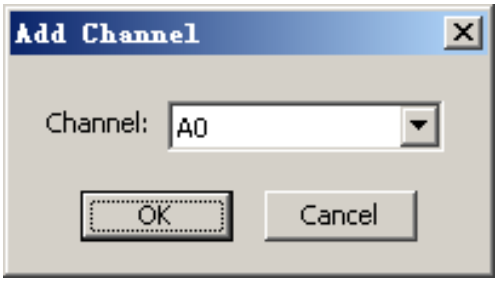
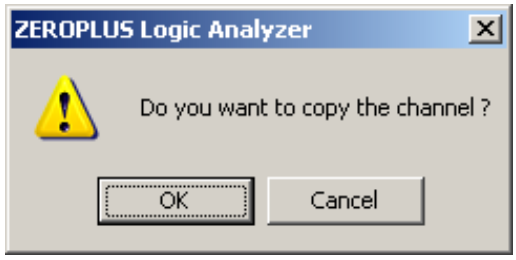
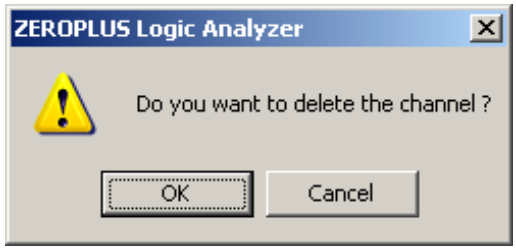
Fig 3-87: **Help** Menu

Menu Bar: **Help**

Menu Item	Detail Menu & Dialog Box
ZEROPLUS Logic Analyzer Help F1	Fig 3-88: Open ZEROPLUS **Logic Analyzer Help** file.
Keyboard Map	 Fig 3-89: The table of **Keyboard Map**.
Report a Problem	Report a problem to our company at: service_2@zeroplus.com.tw
About ZEROPLUS Logic Analyzer	 Fig 3-90: Copyright **About ZEROPLUS Logic Analyzer**.

Open the website of **ZEROPLUS** to know more modules.

Right Key

Menu Item	Detail Menu & Dialog Box
Right-key Menu on Bus/Signal Column **Tip:** The Right-key menu is added on the basic of the Bus / Signal Menu Bar. So the functions of Sampling Setup, Channels Setup, Group into Bus, Ungroup from Bus, Format Row, Rename, ect. are the same as those in the Menu Bar.	 Fig 3-91: Right-key Menu
	 Fig 3-92: Add the required channel in the Bus/Signal column
	 Fig 3-93: Copy the selected channel in the Bus/Signal column
	 Fig3-94: Delete the selected channel in the Bus/Signal column

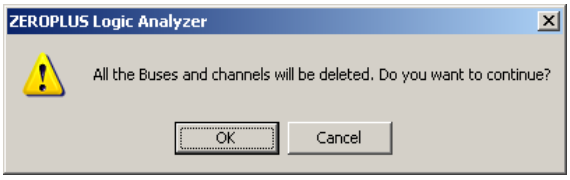


Fig 3-95: Delete all the Buses and channels in the Bus/Signal column

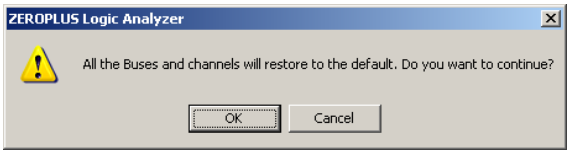


Fig3-96: Restore the deleted Buses and channels in the Bus/Signal column

Right-key Menu on the Waveform Area

Tip:

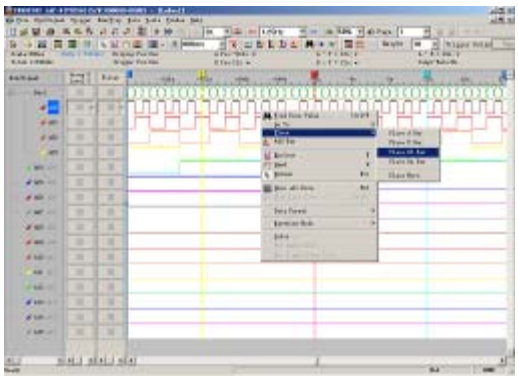
Some functions of the Right-key menu on the waveform area is similar to those in the Data menu of the Menu Bar.

This version adds the functions, such as Place Ds and Dp, Add Bar on the waveform area, and so on.

Fig3-97: Right-key Menu on the waveform Area

The Right-key menu on the waveform area adds the function of Place Ds Bar and Place Dp Bar. However, the functions are only used after the Ds and Dp Bars are activated, otherwise they will be disabled. These functions are the same as those of A Bar.

When the mouse is stopped at a



special position, click the right key on the mouse, select the Place Ds Bar or Place Dp Bar, the Ds or Dp Bar will move to the special position. For example, open "Select an Analytic Range", select the special position, "-10", and then select "Place Ds Bar". See the figure in the right column.

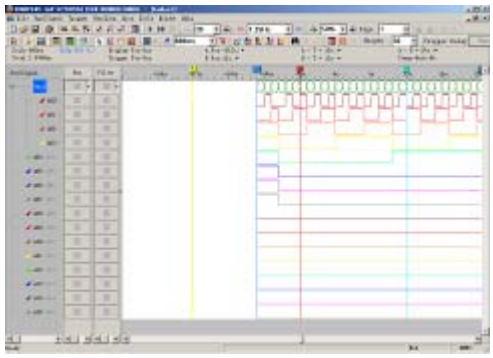
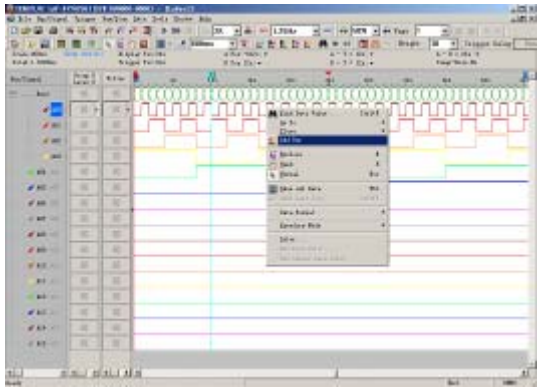


Fig3-98: Place Ds Bar

Tip:

When the mouse is located at a special position on the waveform area, click the right-key to select the Add Bar function; a new Bar will be added automatically in the special position according to the sequence of the letter and color. See the C Bar in the position, "30", in the right column.



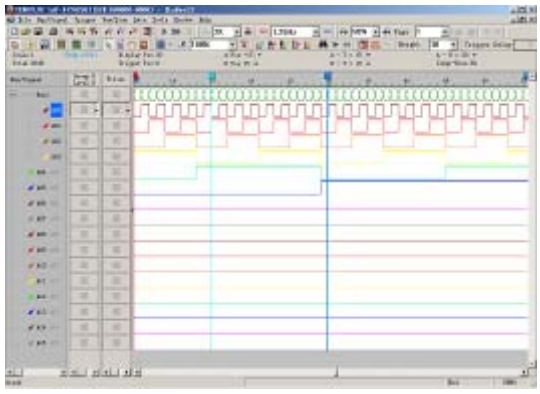


Fig3-99: Add Bar on the waveform area

More Functions on the Waveform Operation Area

Tip:

When the mouse is placed at the name of the current Bar, the Bus state data which belong to the Bar in the current position will be displayed. See the image in the right column.(the data of A Bar in the position of Port A, Port B, Port C and Port D are respectively 0X00F9, 0X0000, 0X0000 and 0X0000).

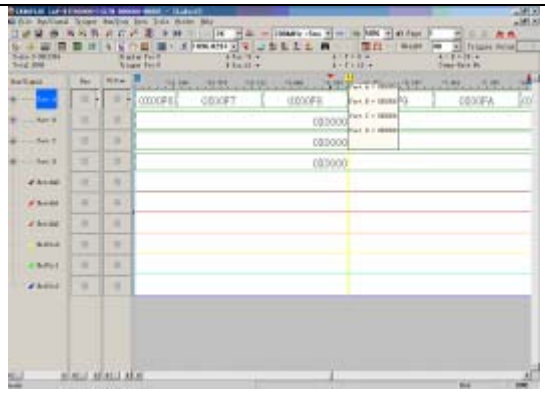


Fig-100: Display the Bar State window

Tip:

The function of Bar Width and Connection Settings can be used by the Bar with the **Ctrl** key, and the way of using those functions are the same as the function of the file check in WINDOWS. Click the **Ctrl** key and the connected Bar synchronously, then double-click the Bar; the Bar Width and Connection Settings dialog box will appear. And the Bar connection function can be activated by the dialog box, and the width between bars can be set as users' requirements. After finishing those operations, many bars can be moved at the same time.

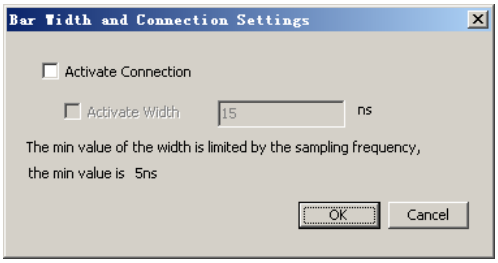


Fig-101: Bar Width and Connection Settings Dialog Box

Activate Connection: Select whether activate the function of the Bar connection.

Activate Width: Set the width between the connected bars, and the unit is set as ns.

Fig-3-102: Drag more than Two Bars (The widths between A Bar and B Bar, A Bar and C Bar are set as 15ns.)

Note: When any of the three bars is dragged, the A Bar, B Bar and C Bar will move synchronously.

3.2 Find Data Value

Find Data Value is a very useful tool to help the users to find data on the received signals.

Step 1. Click the Find Data Value icon; the dialog box of Waveform-find will appear.

Step 2. Use the pull-down menu to select the Bus/Signal Name.
The Bus/Signal listed on the pull-down menu represent the status of the Bus/Signal column as shown in Fig 3-103.

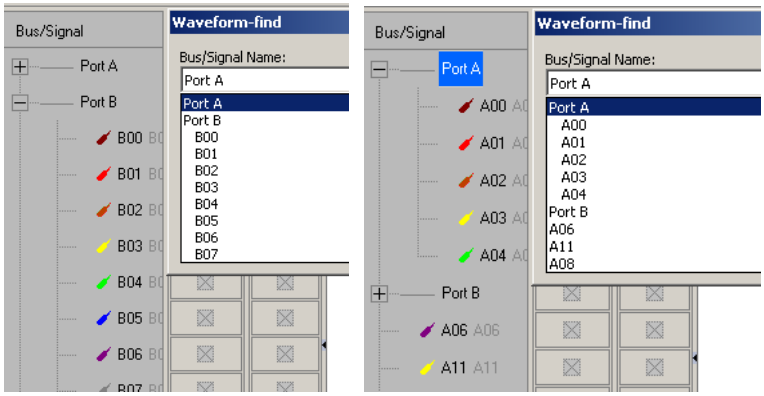


Fig 3-103

Step 3. Choose the character for Find. The list of characters depends on whether it is a Bus, Signal, or the Protocol Analyzer such as IIC/ UART/ SPI…etc that is being searched (see Figs 3-104, 3-105, 3-106, 3-107, 3-108, 3-109, 3-110 and 3-111).

Bus: Choose among =, !=, In Range and Not In Range (enter the MinPosition value or the MaxPosition value).

Protocol Analyzer: Choose the segments of the Protocol Analyzer (enter the value for MinPosition or MaxPosition).

Signal: Choose among Rising Edge, Falling Edge, Either Edge, High and Low.

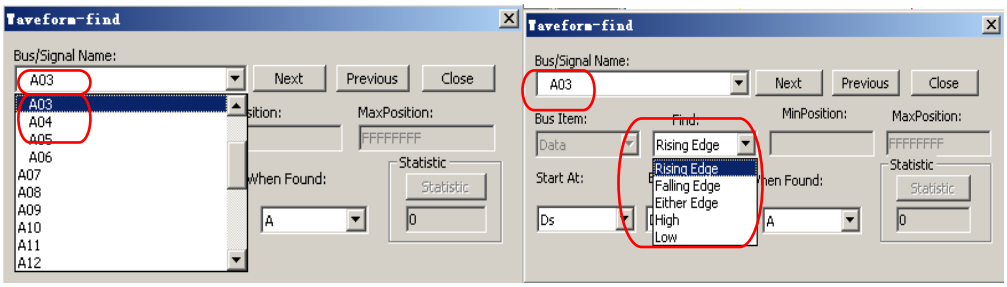


Fig 3-104: Waveform-find Dialog Box of the Logic Signal

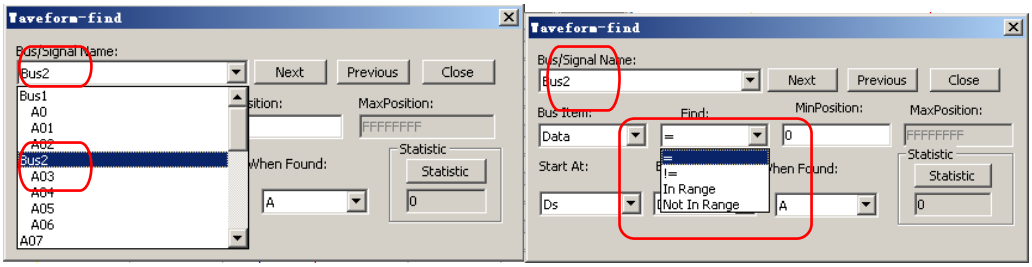


Fig 3-105: Waveform-find Dialog Box of the Logic Bus

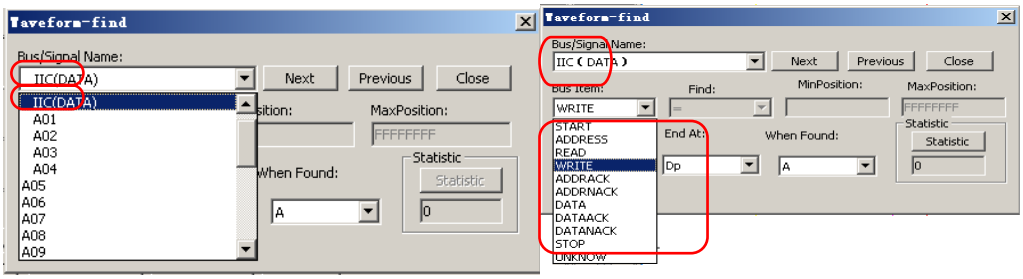


Fig 3-106: Waveform-find Dialog Box of the Protocol Analyzer IIC

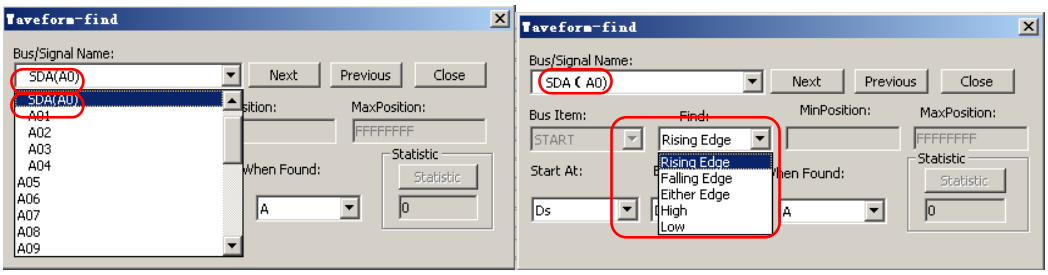


Fig 3-107: Waveform-find Dialog Box of the IIC Signal

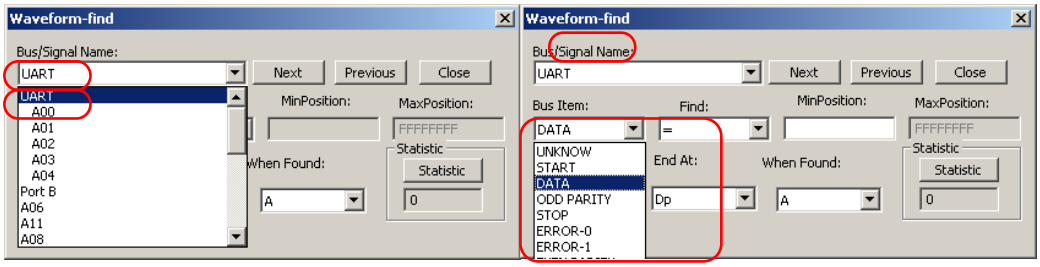


Fig 3-108: Waveform-find Dialog Box of the Protocol Analyzer UART

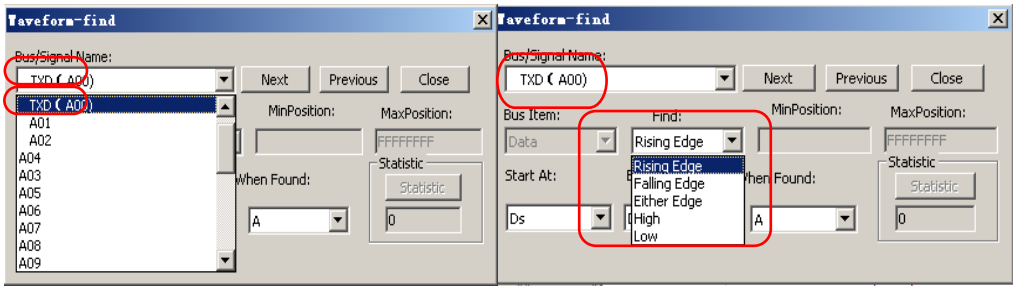


Fig 3-109: Waveform-find Dialog Box of the UART Signal

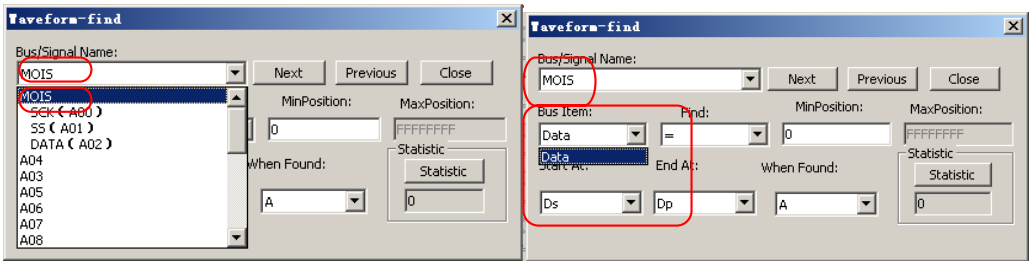


Fig 3-110: Waveform-find Dialog Box of the Protocol Analyzer SPI

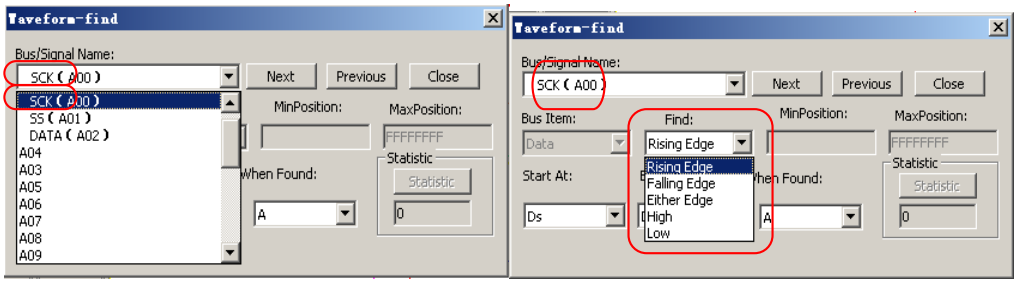


Fig 3-111: Waveform-find Dialog Box of the SPI Signal

Step 4. Choose the position to start the search by selecting one of the following:
Start At: Ds T, A, B, C; **End At:** Dp, A, B, C (select from the pull-down menu), then click **Next** or **Previous** to search it.

When Found: Choose a Bar to mark the result: A, B, C, and other Bars (if available, select from the pull-down list)

Step 5. Click Statistic to show the number of the search results.

Note: It is available only when searching through a Bus.

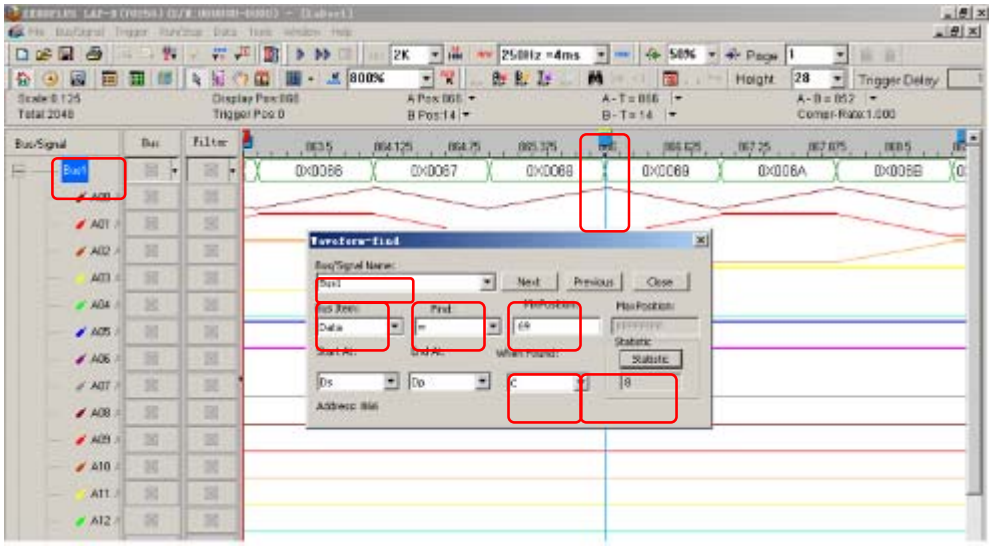


Fig 3-112: The C Bar is placed at the 0X69 of Bus1 where the condition of the Waveform-find is set. The Statistic of the Waveform-find is "8".

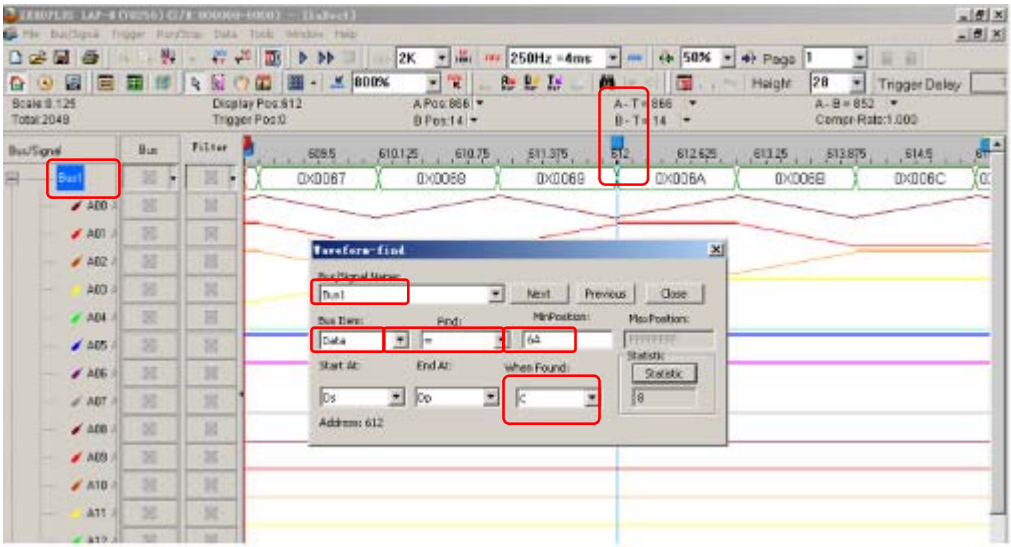


Fig 3-113: The C Bar is placed at the 0X6A of Bus1 where the condition of the Waveform-find is set.

3.3 Statistics Feature

Section 3.3 presents detailed information on the **Statistics** feature in the software interface. The **Statistics** feature presents users information pertaining to nine periodicities: **Integrated Periodicities**, **Positive Periodicities**, **Negative Periodicities**, **Eligible Integrated Periodicities**, **Eligible Positive Periodicities**, **Eligible Negative Periodicities, Start Position, End Position** and **Selected Data**.

Click on the **Statistics** icon . and an interface like. Fig 3-114 *or* Fig 3-115 will pop up.

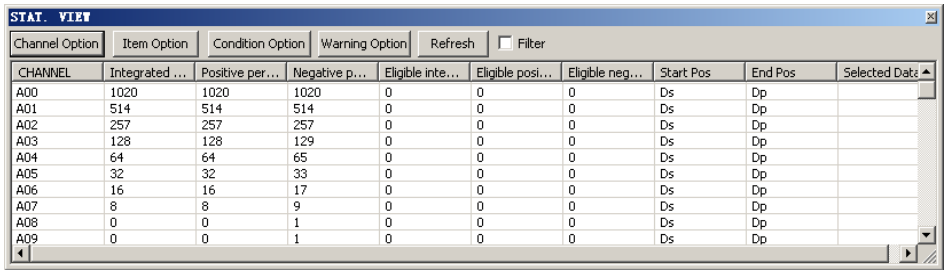


Fig 3-114: **STAT. VIEW**.

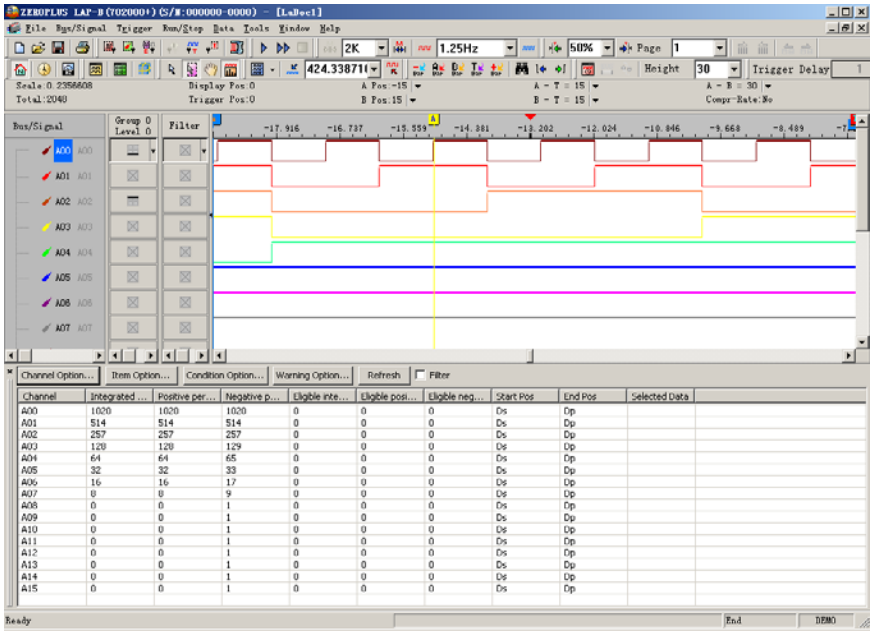


Fig 3-115: Logic Analyzer with Statistics function.

There are four options for adjusting how statistical information may be presented. These four options are **Channel Option**, **Item Option**, **Condition Option** and **Warning Option**.

Channel Option

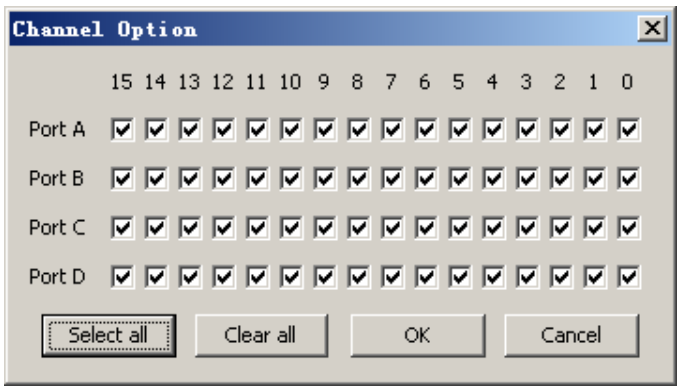


Fig 3-116: **Channel Option**. Allow the choice of pins in which port will be included in the statistical analysis of a test run.

Item Option

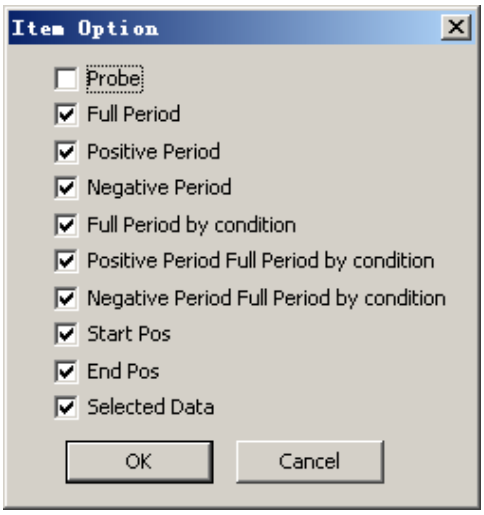


Fig 3-117: **Channel Option**. Allow the choice of periodicities that will be considered in the statistical results.

Conditions Option

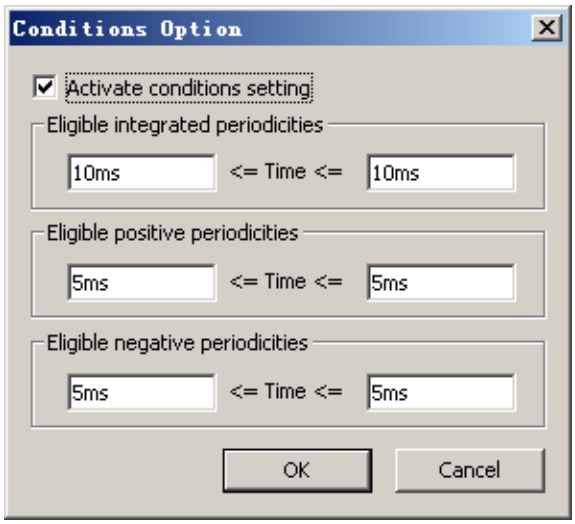
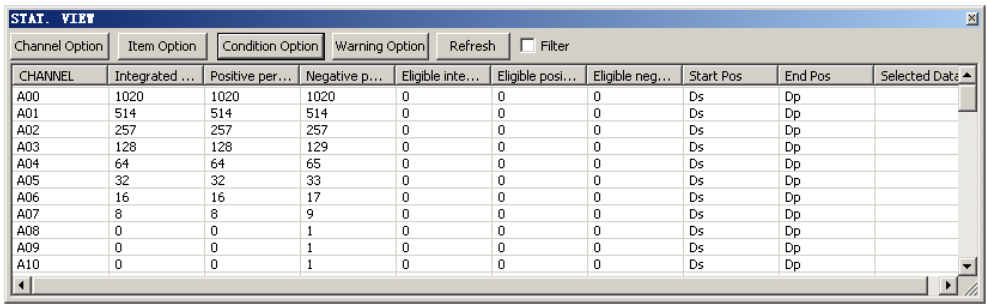


Fig 3-118: **Conditions Option.** Allow the setting of time intervals for Eligible Integrated, Eligible Positive and Eligible Negative Periodicities.



CHANNEL	Integrated ...	Positive per...	Negative p...	Eligible inte...	Eligible posi...	Eligible neg...	Start Pos	End Pos	Selected Data
A00	1020	1020	1020	0	0	0	Ds	Dp	
A01	514	514	514	0	0	0	Ds	Dp	
A02	257	257	257	0	0	0	Ds	Dp	
A03	128	128	129	0	0	0	Ds	Dp	
A04	64	64	65	0	0	0	Ds	Dp	
A05	32	32	33	0	0	0	Ds	Dp	
A06	16	16	17	0	0	0	Ds	Dp	
A07	8	8	9	0	0	0	Ds	Dp	
A08	0	0	1	0	0	0	Ds	Dp	
A09	0	0	1	0	0	0	Ds	Dp	
A10	0	0	1	0	0	0	Ds	Dp	

Fig 3-119: The numbers of waveforms qualified by the set conditions.

Warning Option

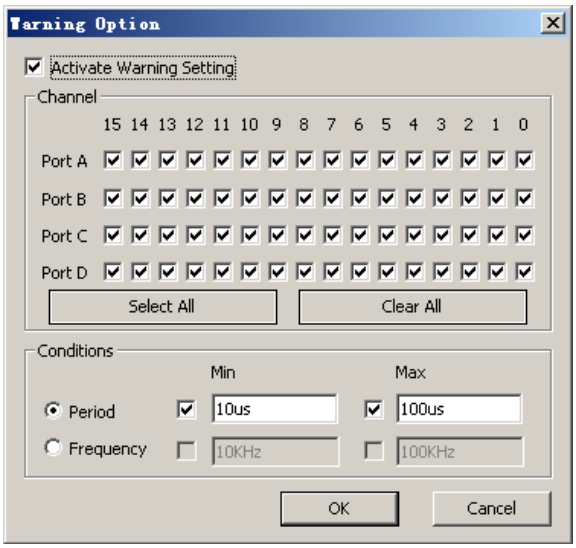


Fig 3-120: **Warning Option.** Allow the choice of pins and ports which will be warned if the conditions are coincident.

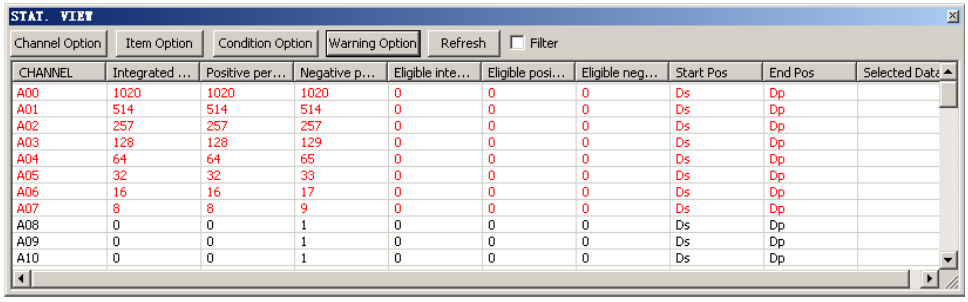


Fig 3-121: The numbers of waveforms qualified by the conditions of the Warning Option are printed in black, otherwise in red.

3.4 Customize Interface

Section 3.4 presents detailed instructions pertaining to how to **modify** the Position **Display Area Data Mode**, how to **modify** the **Ruler Mode**, how to **modify** the **Waveform Height**, and how to **modify** the **Correlated Setting.**

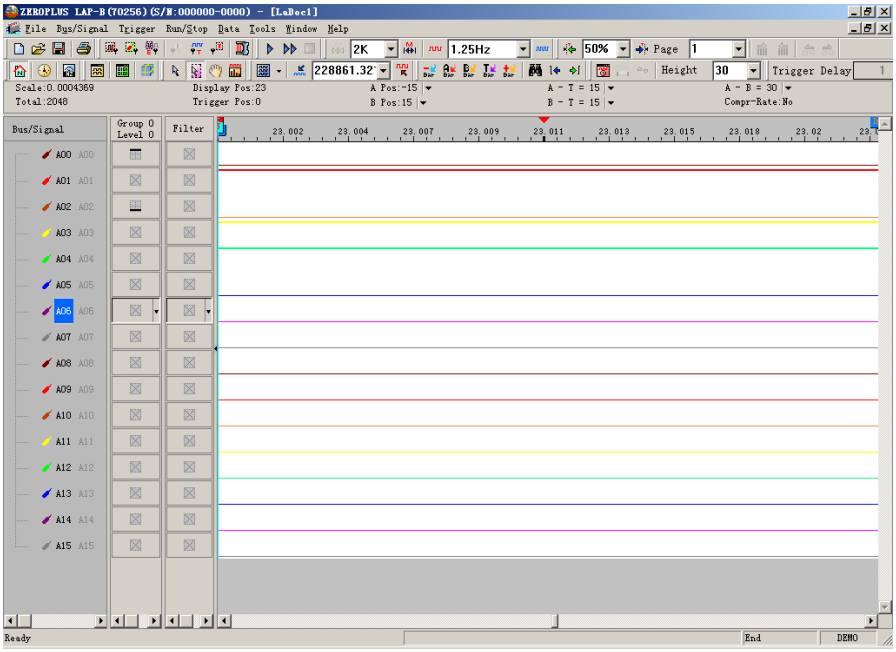


Fig 3-122: The Interface layout Shown in Default Settings.

3.4.1 Modify Display Mode

To modify the display mode, users can use icons on the tool bar / box, or menu.
For the menu, go to **Tools** and click **Customize**. See *Fig.3-126*.

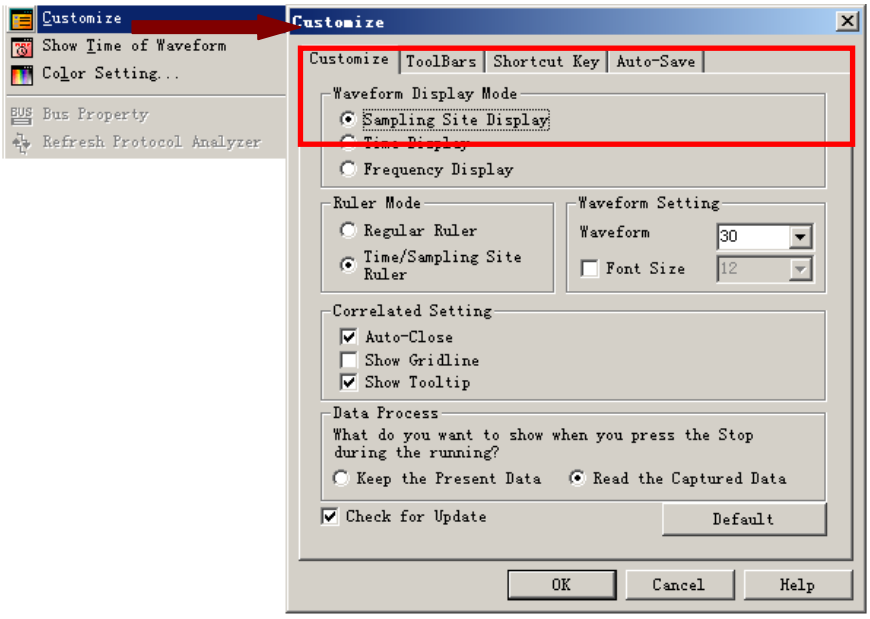
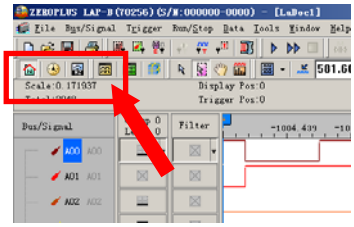


Fig 3-123: Customize the display mode by using the tool bar



Sampling Site Display

Time Display

Frequency Display

Fig 3-124– Tool bar

Fig 3-125 – Toolbar detail

Position Display Area Data Mode – There are 3 modes to determine the method of capturing data from sampling: Sampling Site Display, Time Display and Frequency Display.

3.4.2 Modify Ruler Mode

Use the menu to modify the Ruler Mode.

Go to **Tools** and click **Customize**. See *Fig. 3-126:*

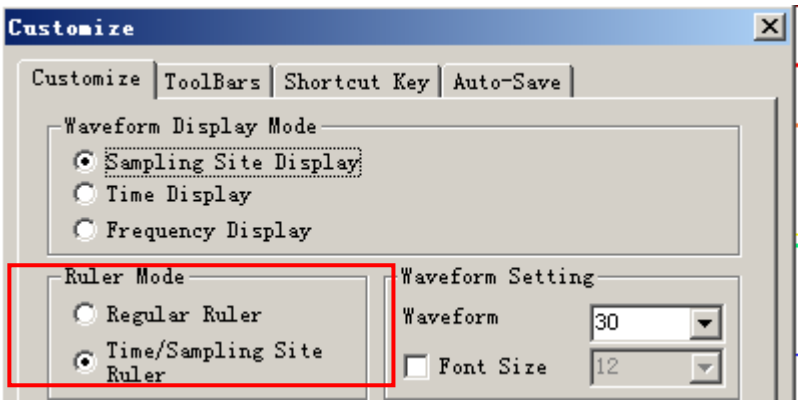


Fig 3-126: Ruler Mode

Regular Ruler

Fig 3-127: Ruler in Regular Ruler

Time/Sampling Site

Fig 3-128: Ruler in Time/Sampling Site

Ruler Mode – There are two styles of Ruler: (Regular Ruler, Time/Sampling Site Ruler).

Regular Ruler:

Present in increments of 5.

Time/Sampling Site Ruler(default):

Present in increments of 50us.

3.4.3 Modify Waveform Height & Correlated Setting

To modify Waveform Height, click **Tools ➔ Customize**.

Waveform Height sets the height of the waveform (18-100) in chosen items at toolbar that will show the amplitude of the waveform.

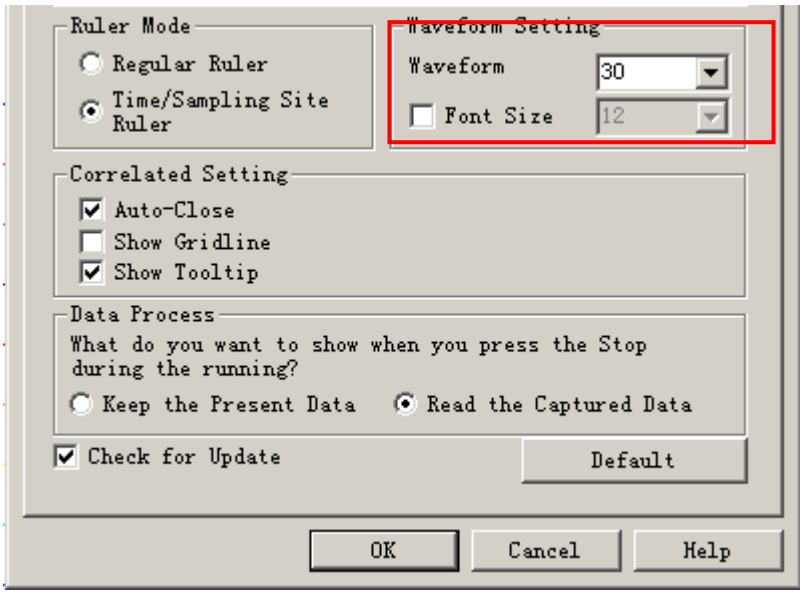


Fig 3-129: Waveform Setting

Waveform Height = 18

Fig 3-130-1

Waveform Height = 40

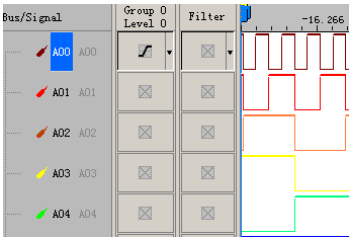


Fig 3-130-2

Fig 3-130 – Examples of Waveform Height

Correlated Setting

Check the boxes to activate the following settings.

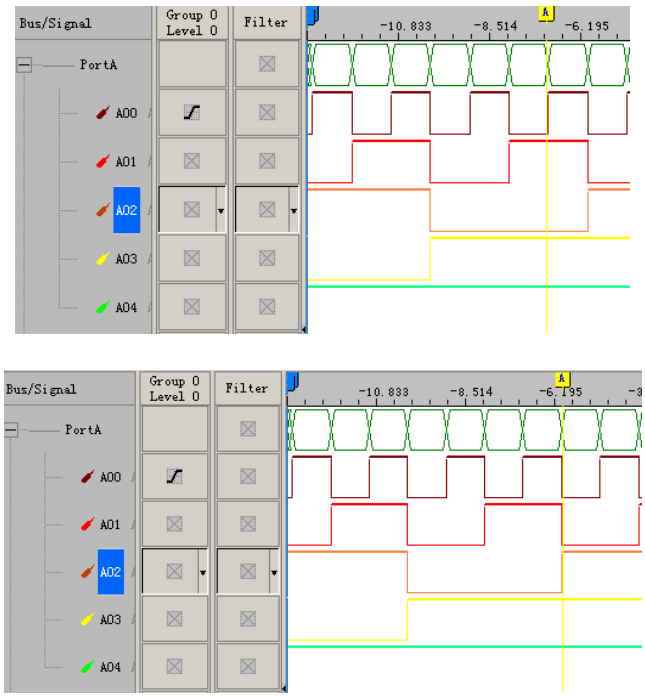


Fig 3-131: An Example for Auto-Close

Auto-Close - With the cursor in the channel, when users try to drag a Bar, the Bar will stop at the approaching edge of the channel (High Edge or Low Edge).

Tip: In the above example, when dragging the A Bar, the A Bar will stop at the Low Edge of A02.

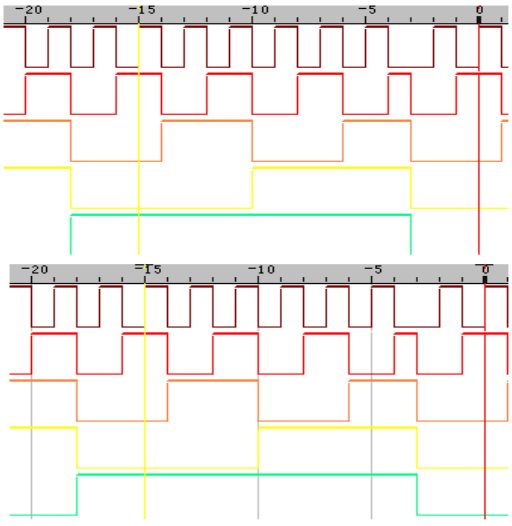


Fig 3-132: Gridlines

Show Gridline - The gridline will be displayed in the waveform display.

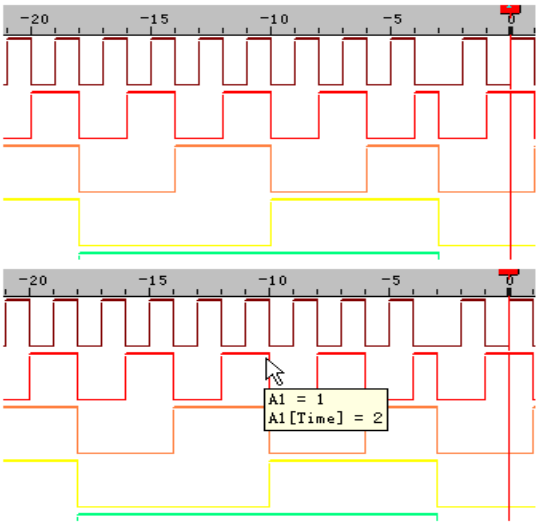


Fig 3-133: Tooltips

Show Tooltip – Leave the mouse over an icon or a waveform and the description will be shown.

Check for Update: The Logic Analyzer software will automatically check for updates when being started.
Default: All the settings of the Customize return to the initial settings.

3.5 Auto-Save

To save captured data for a long time, users can use icons on the tool bar/box, or the menu.

For the dialog box, go to **File** menu to click **Auto Save** or go to **Tools** bar to select **Customize** and select **Auto-Save.** See *Fig.3-134*.

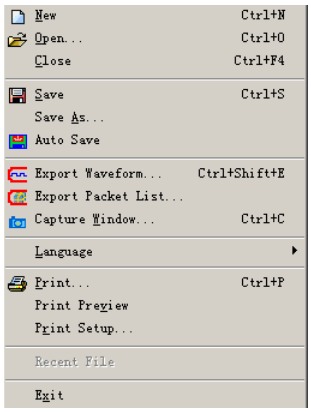


Fig3-134-1: Auto Save on File Menu

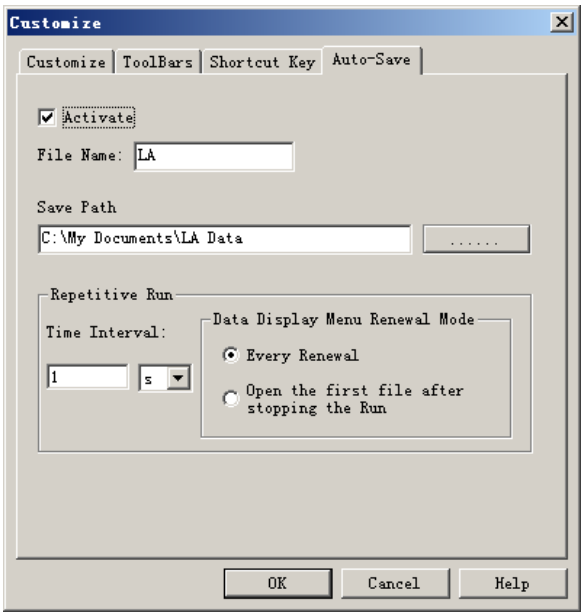


Fig3-134-2: Auto-Save of Customize

Auto-Save: The default is not activated; after activating, it keeps working and users also can choose **Cancel** to close it.

Activate: The default is not activated; after activating, it keeps working and users also can choose **Cancel** to close it.

File Name: Before users name the file, the file name is defaulted as LA. In fact, the saved file name can add a serial number for the file automatically.

Save Path: Users can enter the path directly or choose the path from the selectable path button

.

Time Interval: When the Auto-Save function is activated, the time interval from one finished sampling to the next activated sampling can be set according to users' requirements; the default is 1s, and the unit can be selected from s(second), m(minute) and hr(hour).

Every Renewal: When Repetitive Run is activated, the wave form image or the state image will renew again and again.

Open the First file after stopping the Run: When the Repetitive Run function is activated, the waveform only displays the first file and it isn't renewed; when the Repetitive Run is stopped, the waveform still displays the first file.

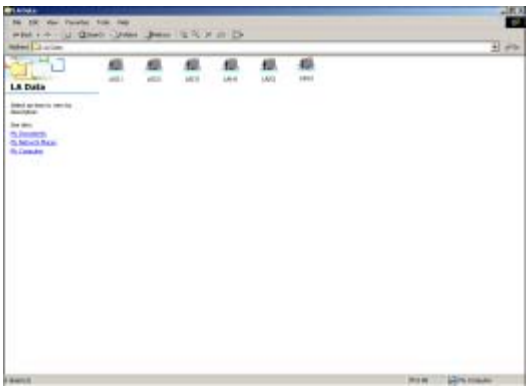


Fig3-135: Auto Save

3.6 Color Setting

To modify **Color**，click **Tools->Color Setting**

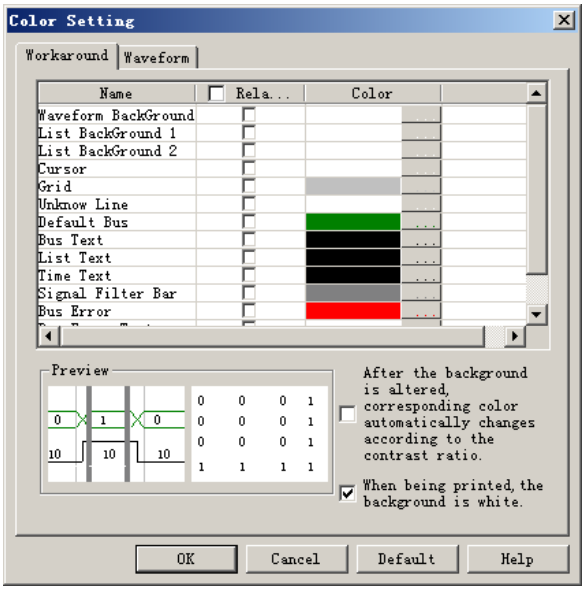


Fig 3-136: Workaround and Waveform Setting

Workaround Color – The workaround color of the Logic Analyzer and the text.

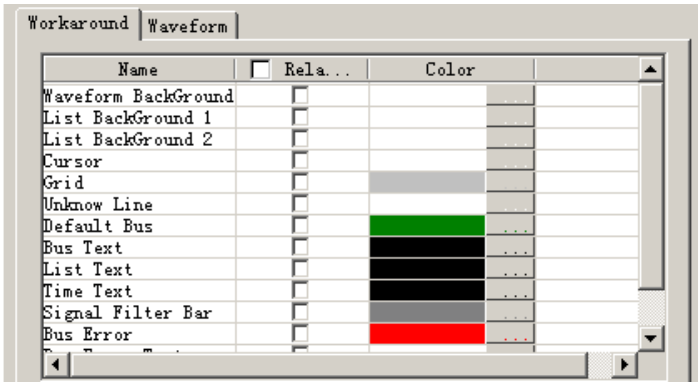


Fig 3-137: Workaround Color Menu

Waveform BackGround: The Logic Analyzer's waveform Viewer BackGround Color.
List BackGround 1: The Logic Analyzer's First Listing Viewer BackGround Color.
List BackGround 2: The Logic Analyzer's Second Listing Viewer BackGround Color.

All optional items include the current color of all Buses, Signals, Cursors , Grids, Unknown Lines, Default Bus, Bus Text, List Text and Time List(users can scroll the vertical wheel to view the selectable items).

Bus Error: Users can configure the color of Bus Error Data from the Color Setting Dialog Box.

Bus Error Text: Users can configure the color of Bus Error Text from the Color Setting Dialog Box.

Relating: When users select one item to change the color of the item, and users want to change other items into the same color; users can select other items at the same time, then the selected items will be changed into the same color. So it is convenient for users to change many items into the same color once.

After the background is altered, corresponding color automatically change according to the contrast ratio – When users set the color for the workaround and have selected the option, the system will switch other colors automatically to become the contrast color.

When being printed, BackGround is white: When being printed, the background color is white.

Waveform – Change the color of the waveforms.

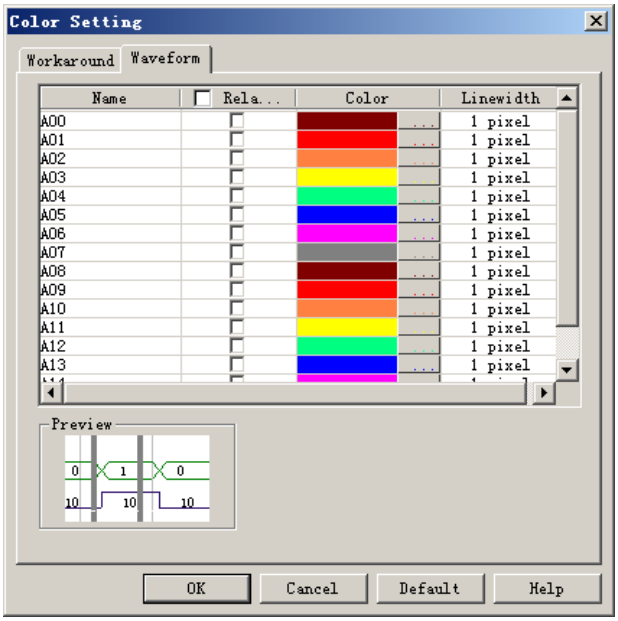


Fig 3-138: Waveform Color Menu

Waveform Color: The channel color can be varied by users.

Linewidth: The linewidth can be adjusted from the pull-down menu; there are three options which are 1pixel, 2pixel and 3pixel.

T
pop

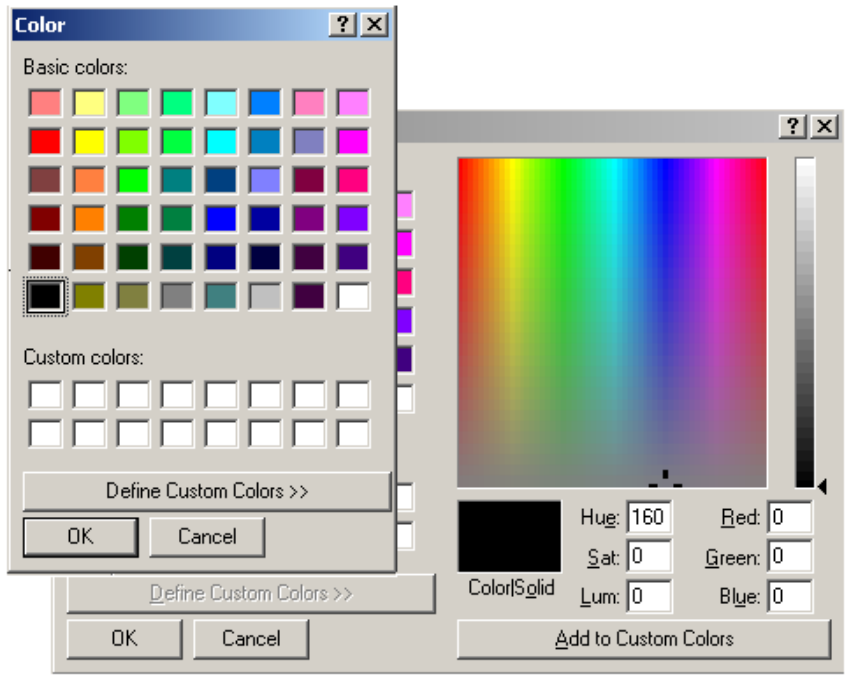


Fig 3-139: **Color** panel with its advanced view.

3.6.2 Modify Waveform Color

Foreground color refers to the color of the output signal lines in the Waveform Display Area. *Fig3-140* presents how to change the color of a signal. Repeat the following procedures if users need to change colors of multiple items.

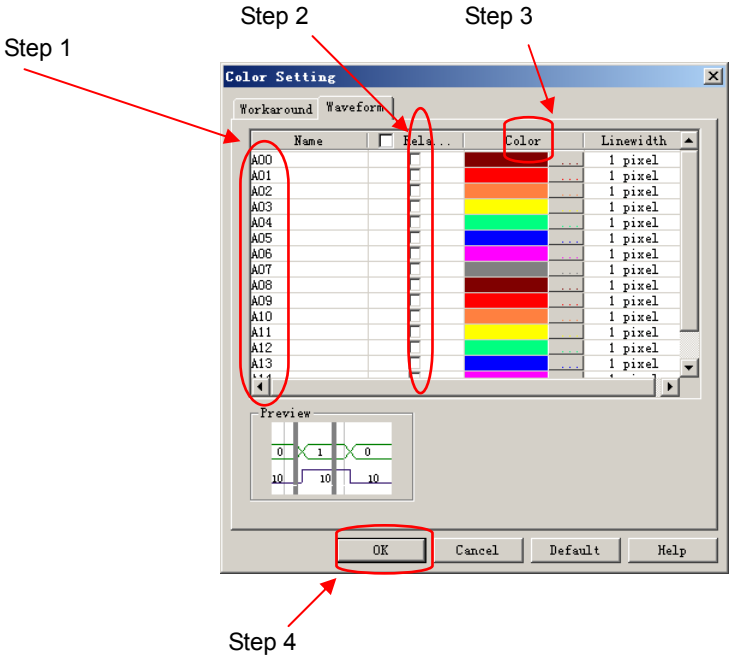


Fig 3-140: Stepwise illustration of changing waveform colors

Step 1: Select several **Optional Items.**

Step 2: Select the corresponding items in **Relating**.

Step 3: Choose a color by following the method shown in Fig 3-139.

Step 4: Click **OK** to change their colors at the same, for example, A01, A02, A03 and A04.

Here is a sample of an altered Logic Analyzer software interface which will be used for further demonstrations in subsequent chapters. See *Fig 3-141:*

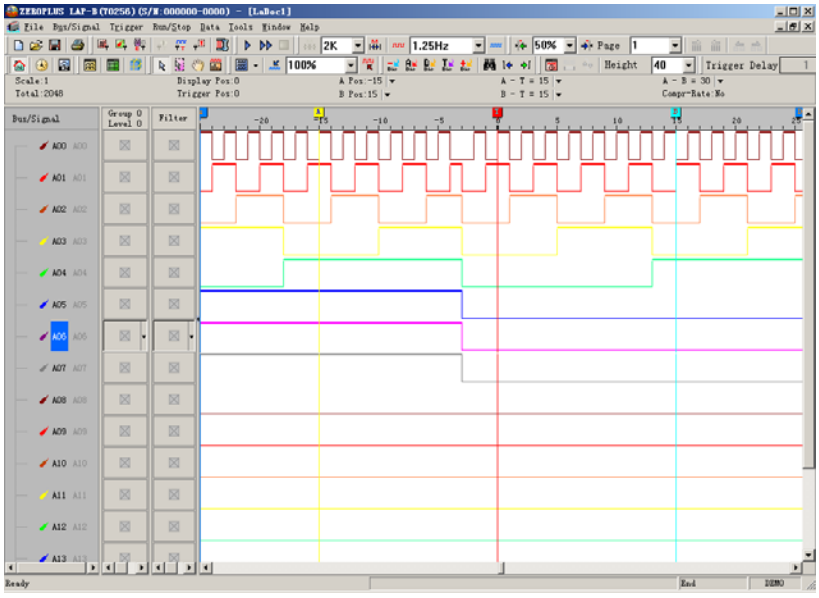


Fig 3-141: An altered interface sample to be used in subsequent chapters.

3.7 The Flow of Software Operation

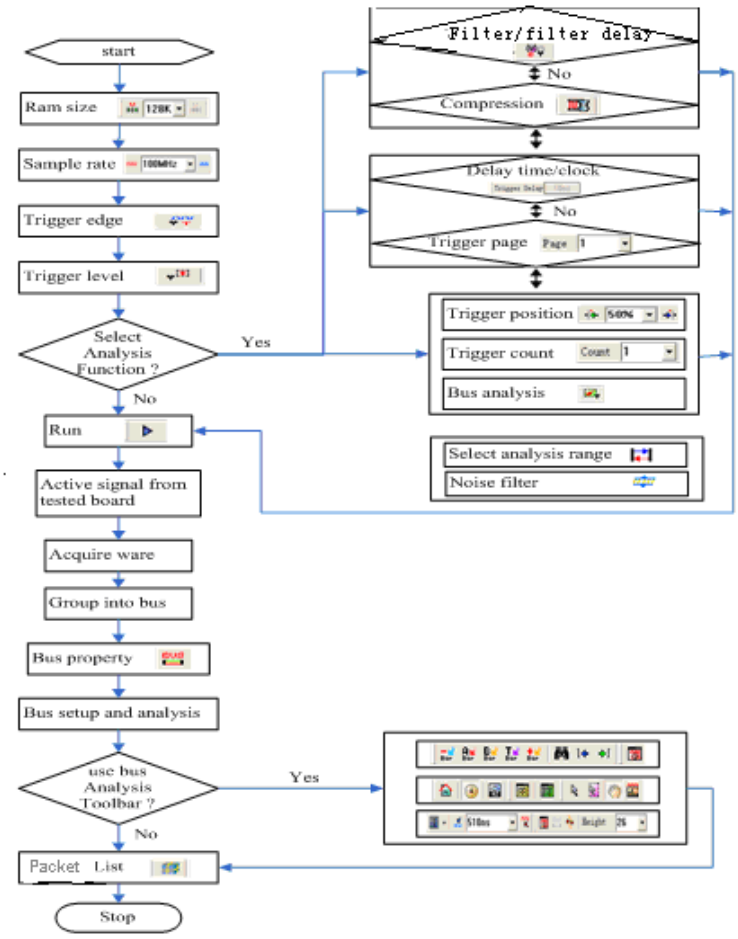


Fig 3-142: Software Flow Diagram

Conclusion

Information demonstrated in this chapter is only for entrance level. There are more advanced approaches which may require fewer steps than those shown in this chapter. This chapter is meant to equip users with sufficient grounding of the Logic Analyzer's software interface.

4 Introduction to Logic Analysis

4.1 The Logic Analysis
4.2 The Bus Logic Analysis
4.3 Plug Analysis
4.4 Bus Packet List
4.5 Bus Analysis
4.6 Compression
4.7 Signal Filter and Filter Delay
4.8 Data Contrast
4.9 Noise Filter
4.10 Refresh Protocol Analyzer

Objective

Chapter 4 gives detailed instructions on performing two basic analysis operations and five advance analysis applications with the Logic Analyzer. These two basic analysis operations are the Logic Analysis and the Bus Analysis, which are fundamental to all further applications. The other five advance analysis applications are the IIC (Inter Integrated Circuit) Analysis, the UART (Universal Asynchronous Receiver Transmitter) Analysis, the SPI (Synchronous Peripheral Interface) Analysis, Compression and Signal Filter and Filter Delay.

4.1 Logic Analysis

Logic Analysis is meant for a single signal analysis. Section 4.1 gives detailed instructions on the software's basic setup.

Basic Software Setup of the Logic Analysis

Task 1. Sampling Setup

Step 1. Click icon or click **Sampling Setup** from **Bus/Signal** on the menu bar, the dialog box as shown in Fig 4-1 will appear.

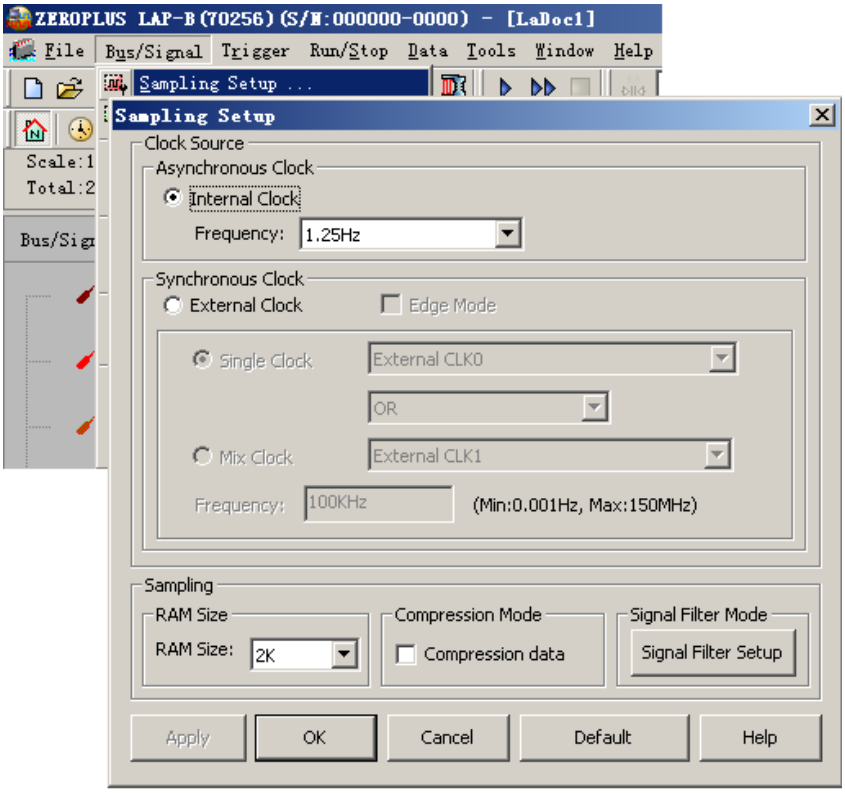
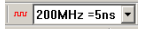


Fig 4-1 – Sampling Setup

Step 2. Clock Source(Frequency)

Internal Clock (Asynchronous Clock)

Click on Internal Clock, and then select the Frequency from the pull-down menu to set up the frequency of the device under test (DUT). The frequency of the Internal Clock must be at least four times higher than the frequency of the Oscillator on the DUT. Or, select the frequency 

from the pull-down menu on Tool Bar as Fig 4-2 shows.

Tip: Connect the output pin of the oscillator from the tested board to the Signal connector of Logic Analyzer to measure its using the internal clock of Logic Analyzer.

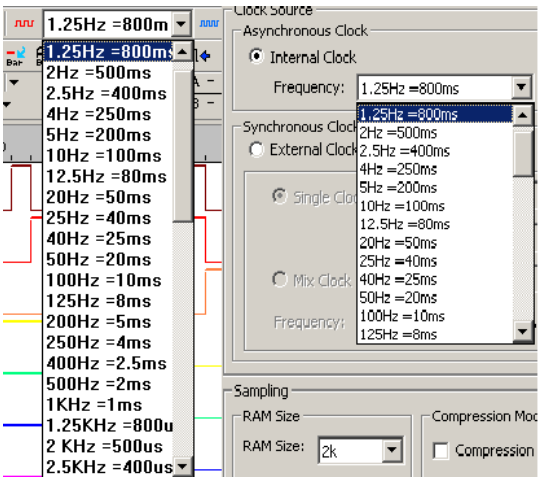


Fig 4-2 – Clock Source Pull-down Menu

External Clock (Synchronous Clock)

Click on External Clock, and then select "Single Clock" or "Mix Clock" to sample the external signals. Users can start the logic operation with the "Single Clock" when they start the "Mix Clock". In the Frequency column, type the frequency of the oscillator on the DUT as shown in Fig 4-3.

Tip: The External Clock is applied when the frequency of the oscillator on the tested board is less then 100MHz. Connect the output pin of the oscillator on the tested board to the CLK pin of Logic Analyzer.

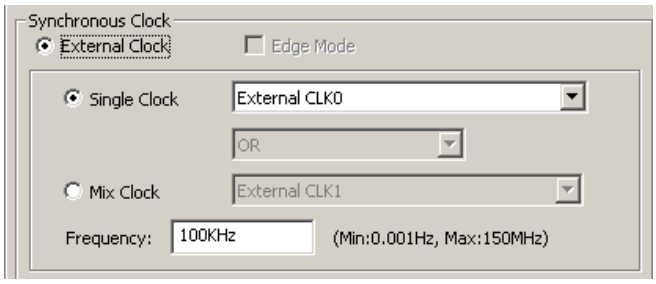


Fig 4-3 - External Clock

Step 3. RAM Size

Click on the RAM Size from the pull-down menu on the Sampling Setup dialog box as shown in Fig 4-4.

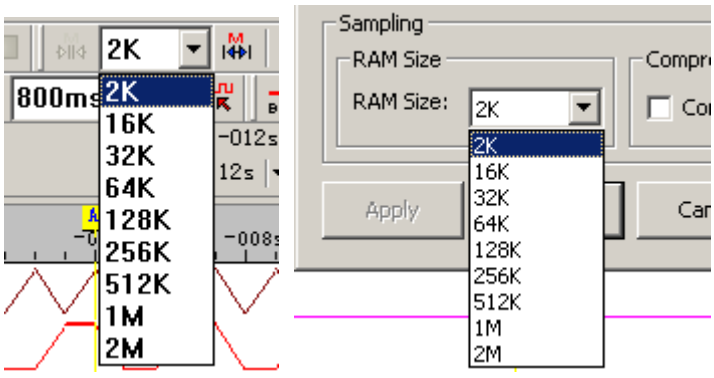


Fig 4-4 – RAM Size

Task 2. Trigger Property Setup

Step 1. Click icon or click Trigger **Property** from the **Trigger** on the Menu Bar. The dialog box will appear as shown in Fig 4-5.

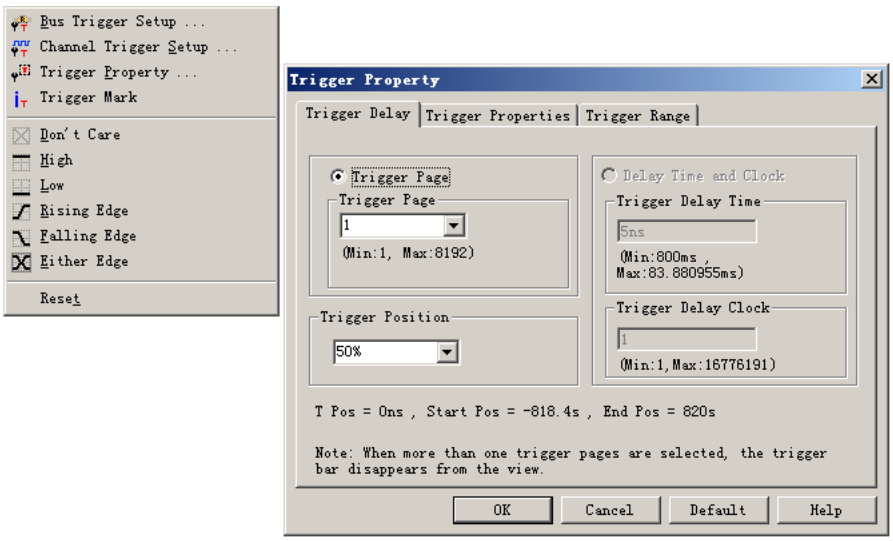


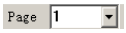
Fig 4-5 - Trigger Properties

Step 2. Trigger Delay Setup

The Trigger Page, the Delay Time and Clock can't be applied at the same time.

Trigger Page:

Click Trigger Page, then type the numbers or select the numbers from the pull-down menu of the Page



on the Tool Bar or click the pull-down menu of the Trigger Page on the "Trigger Delay" page of the Tr igger Property dialog box as shown in Figs 4-6, 4-7 and 4-8. The selected page numbers will be displ ayed on the screen.

Tip: The Trigger Bar (T Bar) will not be displayed when the setup of the Trigger Page is more than 1.

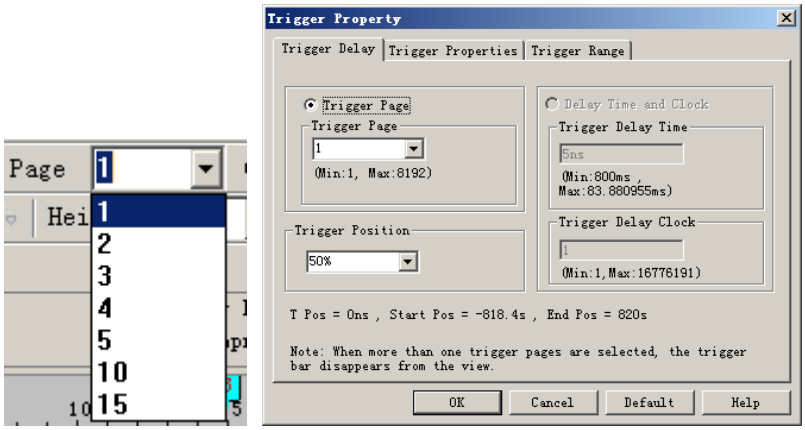


Fig 4-6 – Trigger Page

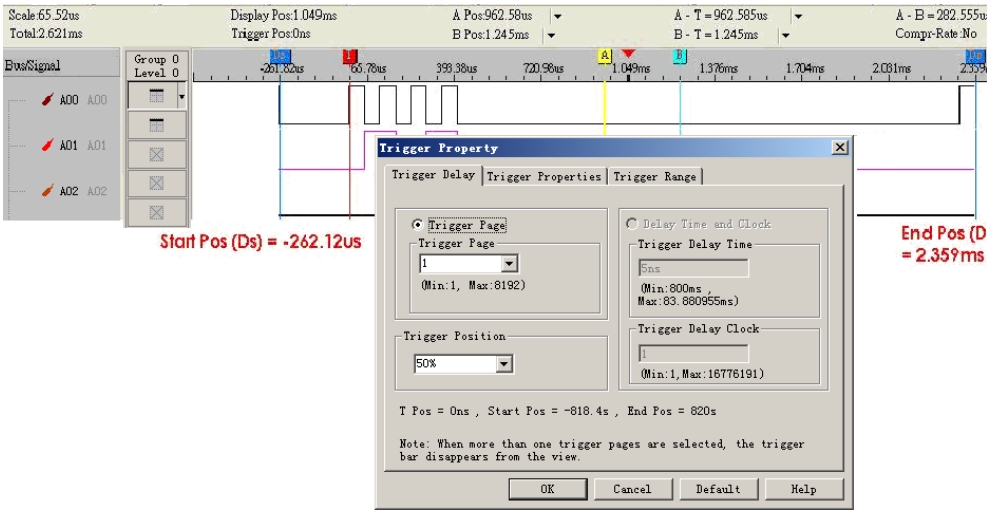


Fig 4-7 – Trigger Page and Screen(1)

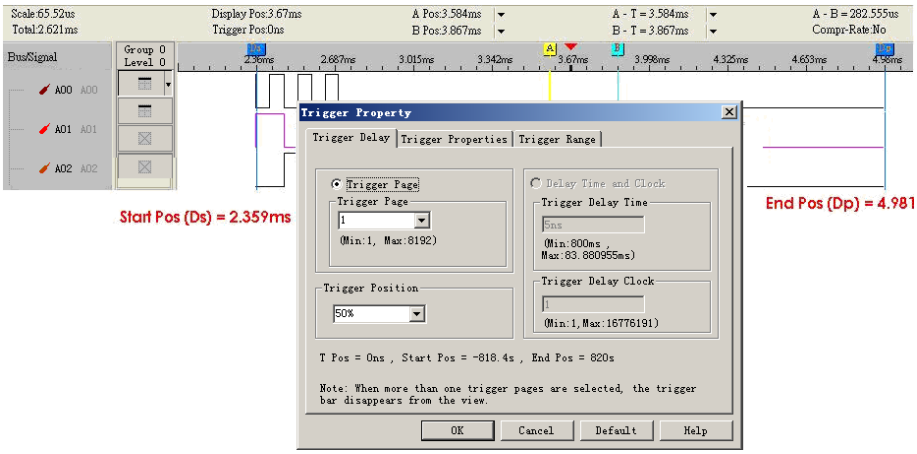


Fig 4-8 – Trigger Page and Screen(2)

Delay Time and Clock:

This function has been disabled in this version.

Trigger Position:

Type the percentages or select the percentages from the pull-down menu of the on the Tool Bar or click the pull-down menu of the Trigger Position on the "Trigger Delay" page of the Trigger Property dialog box as shown in Figs 4-9, 4-10, 4-11and 4-12. The selected Trigger Position percentages will be displayed where the trigger data is counted from the right side of the screen of the system.

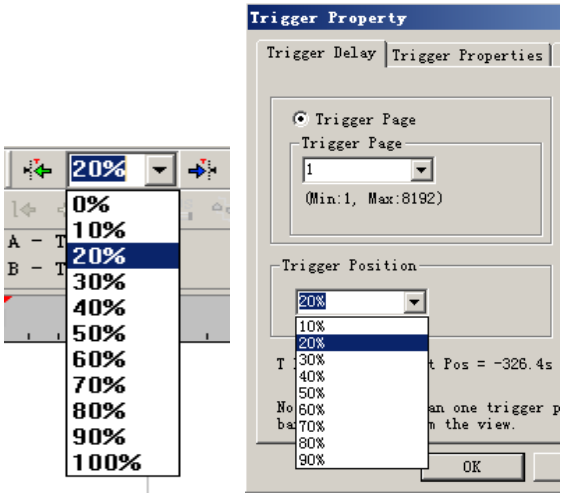


Fig 4-9 – Trigger Position Pull-down Menu

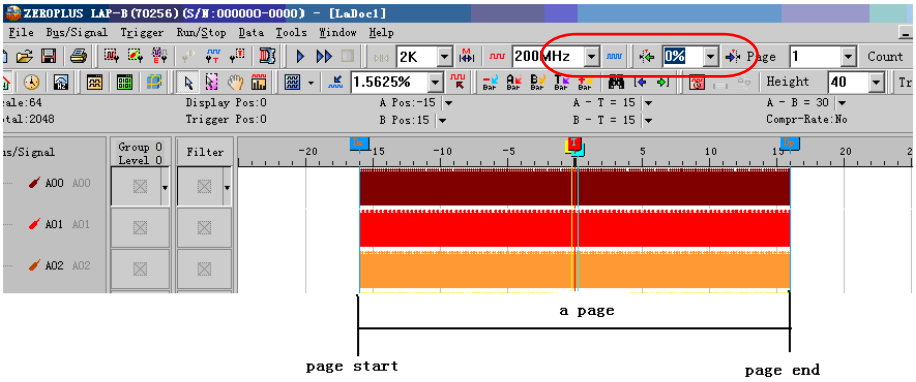


Fig 4-10 – Trigger Position 0%

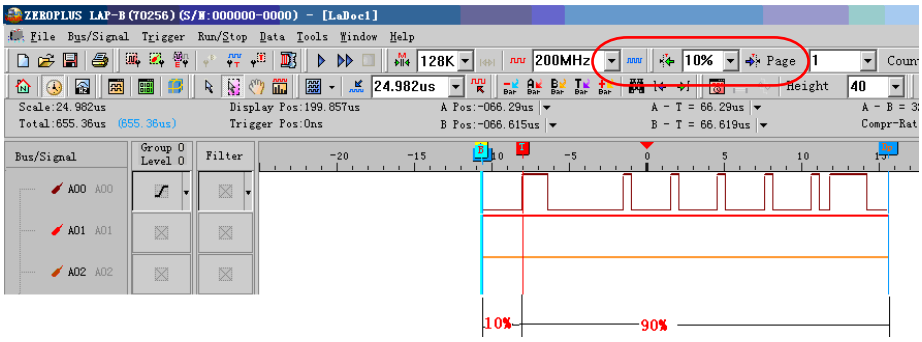


Fig 4-11 – Trigger Position 10%

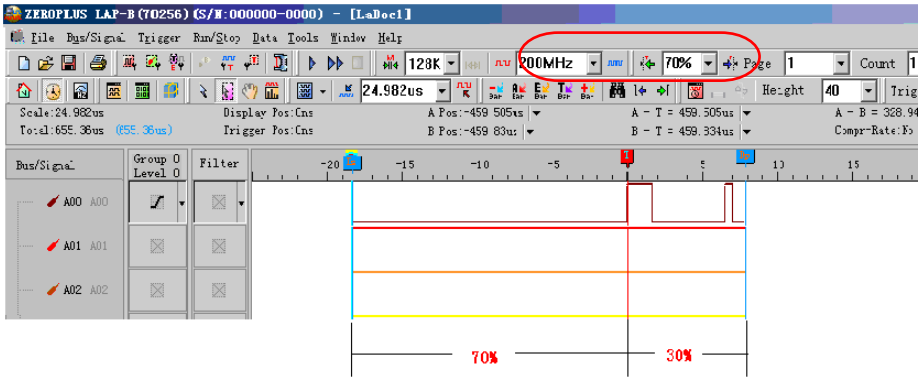


Fig 4-12 – Trigger Position 70%

Step 3. Trigger Voltage Setup

Click the pull-down menu of Trigger Voltage on Port A, B, C and D to select the Trigger Voltage as the voltage level that a trigger source signal must reach before the trigger circuit initiates a sweep.

Tip: There are four commonly used preset voltages for Trigger Voltage, TTL, CMOS (5V), CMOS (3.3V) and ECL. Users also can define their own voltage from -6.0V to +6.0V to fit with their DUT.
Port A represents the pins from A00 ~ A07 on the signal connector of the Logic Analyzer, and so do Port B, C and D. The voltage of each port can be configured independently.

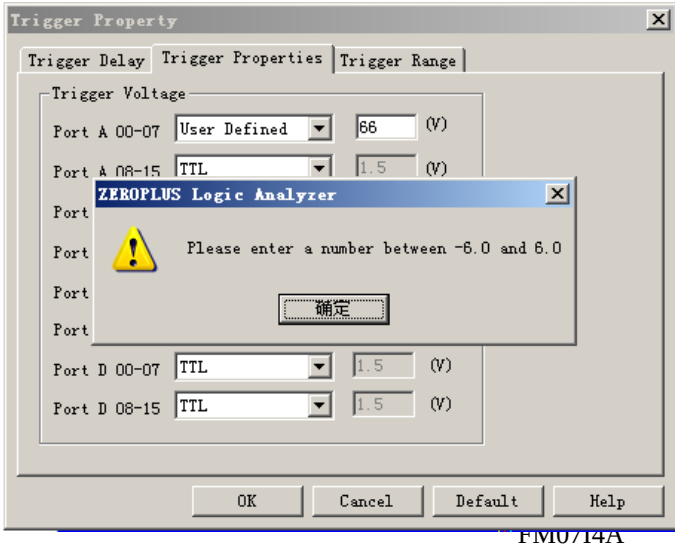


Fig 4-13 – Trigger Properties Error

Step 4. Trigger Range Setup

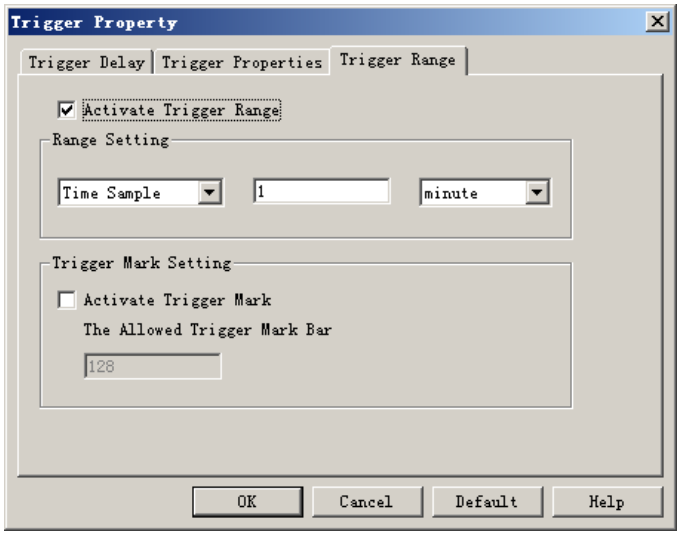


Fig 4-14-Trigger Range

1. **Trigger Range :** The default is not activated.

2. **Range Setting:**

There are "Time Sample" and "Frequency Sample" in the part of Range Setting; the default is "Time Sample". The units of Time Sample are 'second', 'minute', 'hour' and 'day'. The unit of Frequency Sample is 'times'. Users can set the value as their requirements in the editor box.

3. **Trigger Mark Setting:**

Activate Trigger Mark: The number can be set in the range of 0 and 65535; however, the default of the function is non-activated.

Task 3. Bus Trigger and Trigger Mark Setup

Step 1. Click icon or click Bus Trigger and Trigger Mark from the Trigger on the Menu Bar. The menu will appear as shown in Fig 4-15.

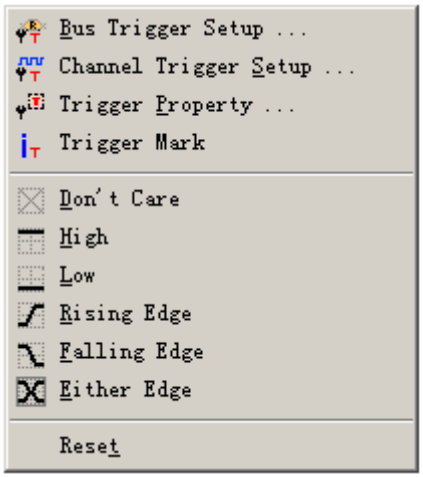


Fig 4-15 -Trigger Menu

Step 2. Bus Trigger Setup

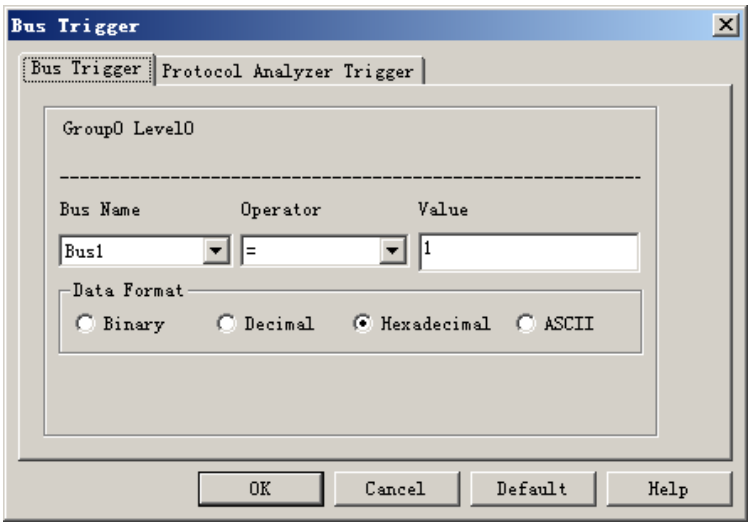


Fig4-16 - Bus Trigger

Tip: The Bus Name item can be selected for the pull-down menu. (It only displays the Bus name) And the ASCII mode also is added.

Step 3. Protocol AnalyzerTrigger Setup

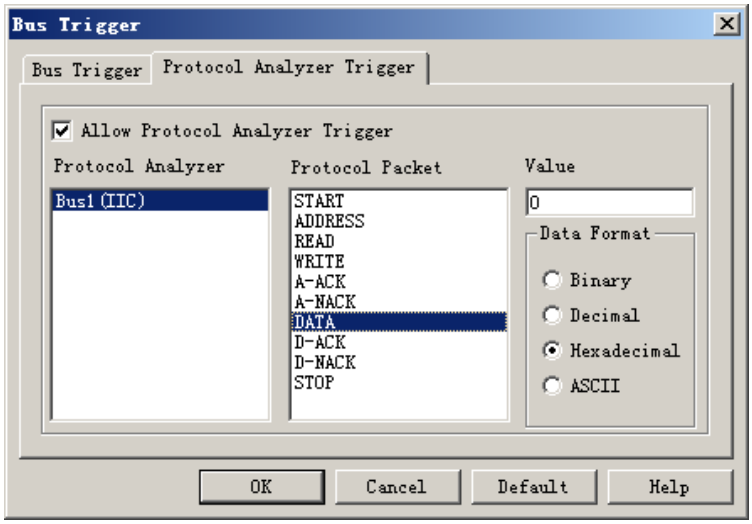


Fig4-17 - Protocol Analyzer Trigger

Allow Protocol Analyzer Trigger: When it is selected, the Protocol Analyzer Trigger function is activated. And then users can set Protocol Analyzer, Protocol Packet, Value and Data Format.

Protocol Analyzer: It only displays the name of the Protocol Analyzer and only one name can be selected.

Protocol Packet: It is displayed according to the data in every Protocol Analyzer.

Value: The value needs to be entered in the frame, and the data mode can be selected according to users requirements; the default is Hexadecimal. When a value can be inputted in the selected Protocol Analyzer data, the frame can be used. Or, the frame will be disabled. For example: Protocol Analyzer IIC, when the Protocol Packet is DATA, the frame can be used, to the contrary, when START of the Protocol Packet is selected, the frame is disabled.

Data Format: The displayed value mode can be selected. There are four options: Binary, Decimal, Hexadecimal and ASCII.

Step 4. Trigger Mark Setup

To find the item in the Bus better, users can activate Trigger Mark function after starting Bus Trigger. The Trigger Mark is shown with T Bar, according to the number of the trigger positions, the T Bar is displayed in order T0, T1, T2, T3, T4……..and the color is red as the image below:

1. Bus: The trigger condition is "0"; the red T Bar marks the trigger condition in order

Fig4-18 - Bus Trigger Mark

2. Protocol Analyzer (IIC): The trigger condition is Data=0; the red T Bar marks the trigger condition in order.

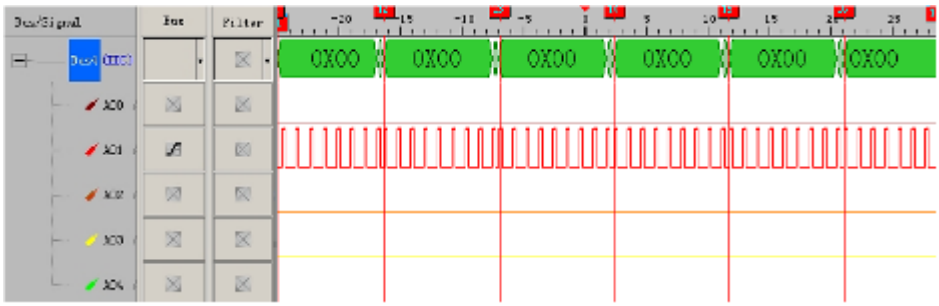


Fig4-19 - Protocol Analyzer Trigger Mark

Task 4. Channel Trigger Setup

Step 1. Click con or click Channel **Trigger Setup** from the **Trigger** on the Menu Bar. The dialog box will appear as shown in Fig 4-20.

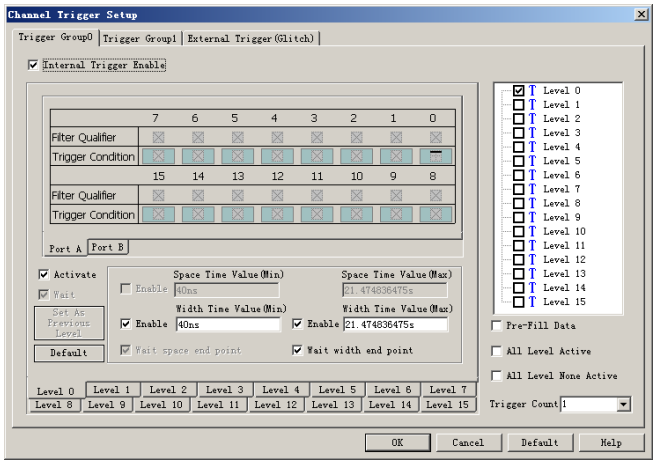


Fig4-20 – Channel Trigger Setup

Step 2. Trigger Count Setup

Type the numbers or click the pull-down menu of the Trigger Count on the Trigger Setup dialog box as shown in Fig 4-21.

The system will be triggered where the Trigger Count is set as show in Figs 4-22, 4-23.

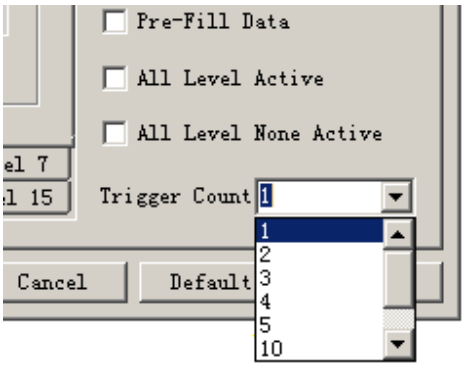


Fig 4-21 – Trigger Count Pull-down Menu

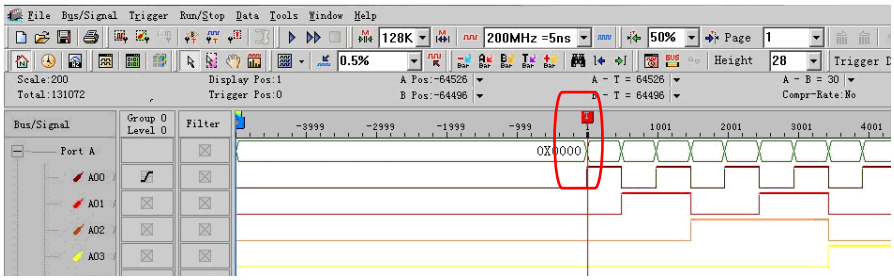


Fig 4-22 – Trigger Count Screen Shot 1

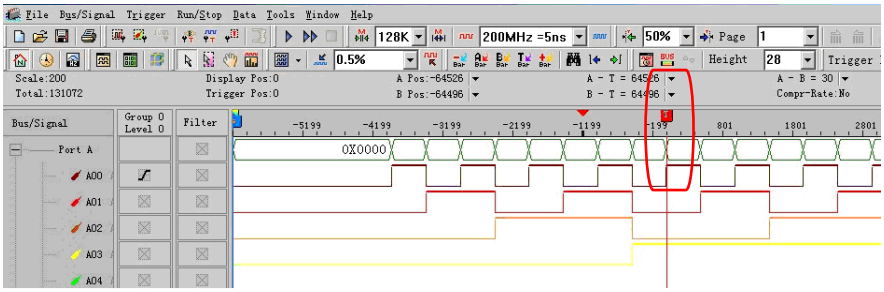


Fig 4-23 – Trigger Count Screen Shot 2

Step 3. External Trigger (Glitch)**:**

Select the **External Trigger (Glitch)** on the **Trigger Setup** dialog box. The **External Trigger (Glitch)** dialog box will appear as shown in Fig4-24.

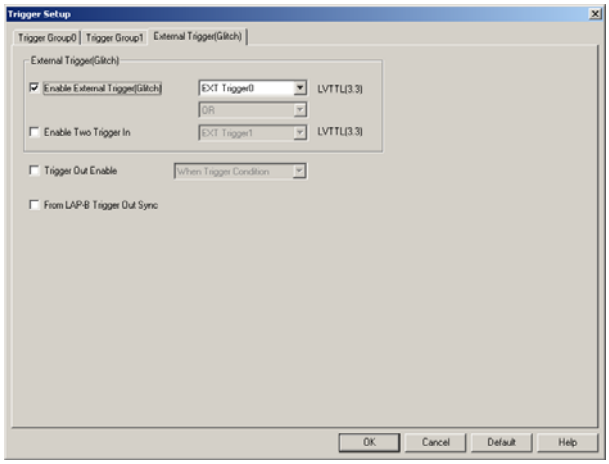


Fig4-24 – External Trigger (Glitch)

Enable External Trigger (Glitch): Activate the first group external trigger. It includes four selections which

are EXT Trigger0, EXT Trigger 1, EXT Trigger 2 and ~ EXT Trigger0.

Enable Two Trigger In: Activate the second group external trigger. It includes four selections which are EXT Trigger0, EXT Trigger 1, EXT Trigger 2 and ~ EXT Trigger1. When you start it , you can start the logic operation with the first one group.

Trigger Out Enable: Set the output trigger condition.

There is an output point for the hardware, and it can be selected by the software (three selections are **When Trigger Condition**, **START** and **STOP**).

From LAP-B Trigger Out Sync: It can accept the trigger signal from another Logic Analyzer.

Task 5. Bus/Signal Trigger Edge Setup

Highlight a designated signal, and then set its required trigger edge.

1. Left Click to set the signal trigger edge as shown in Fig 4-25.
2. Right Click to set the signal trigger edge as shown in Fig 4-26.
3. Click Trigger on the menu bar and choose a trigger edge from the list of triggers as shown in Fig 4-27.

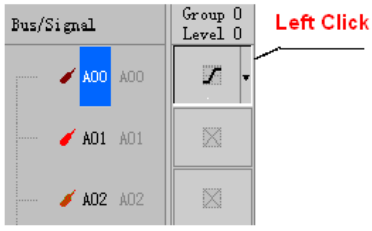


Fig 4-25 – Left Click

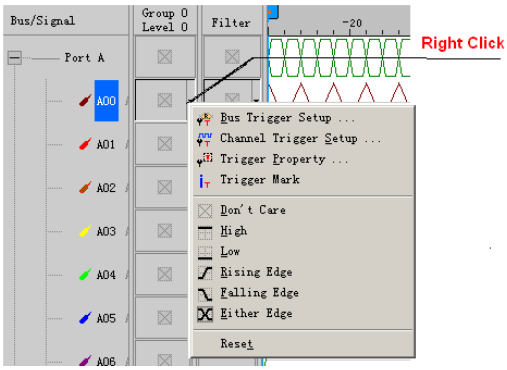


Fig 4-26 – Right Click

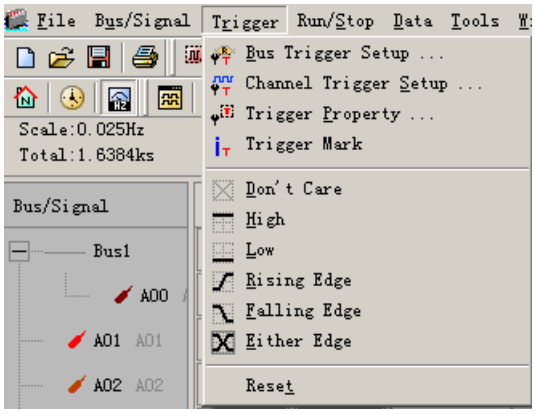


Fig 4-27 – Trigger Menu

Task 6. Run to Acquire Data

Step 1. Single Run

Click the Single Run icon from the Tool Bar or press START button on top of Logic Analyzer (or press F5) or click Single Run from Run/Stop of the Menu Bar, then activate the signal from the DUT to the Logic Analyzer to acquire the data shown in the waveform display area.

Step 2 . Repetitive Run

Click the Repetitive Run icon from the Tool Bar or click Repetitive Run from Run/Stop of the Menu Bar, activate continuous signal to the Logic Analyzer to acquire the continuous data; and then click the Stop icon to end the repetitive run.

Tip: Click icon to view all the data, and then select the waveform analysis tools to analyze the waveforms.

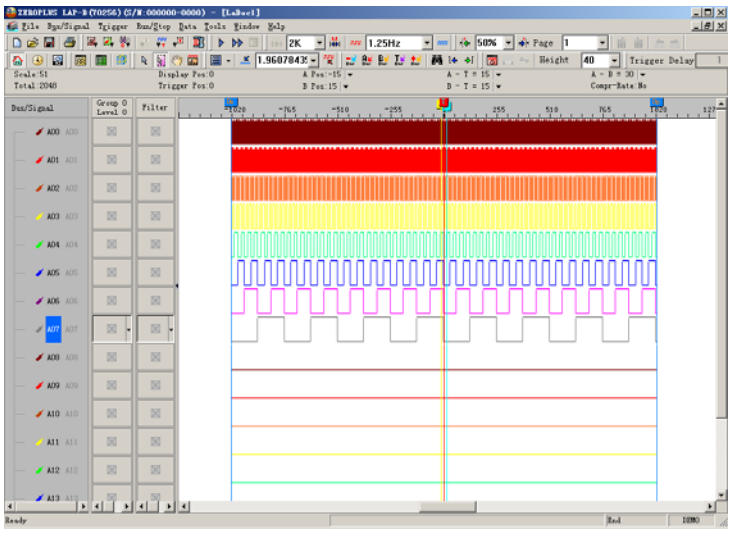


Fig 4-28 – Click icon to view all the data

Step 3. Stop

Click the Stop icon to end the Run.

Tip: If the status is "Waiting…" with no signal output as shown in Fig 4-29, click the Stop icon to end the Run. Check the setup again, and try the Run process again.

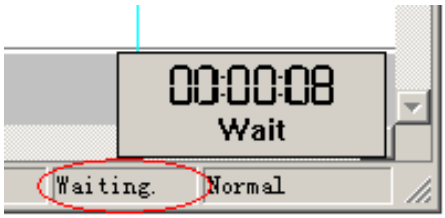


Fig 4-29 – Waiting Status

4.2 Bus Logic Analysis

Section 4.2 presents detailed instructions about logic analysis with a set of grouped signals, which is known as Bus Logic Analysis.

Basic Software Setup of the Bus Logic Analysis

Step 1. Set up the RAM Size, Frequency, Trigger Voltage and Trigger Position as described in Section 4.1.

Step 2. Group channels into a Bus.

Click **Channels Setup** on Bus/Signal of the Menu Bar, or click icon.
The dialog box as shown in Fig 4-30 will appear.

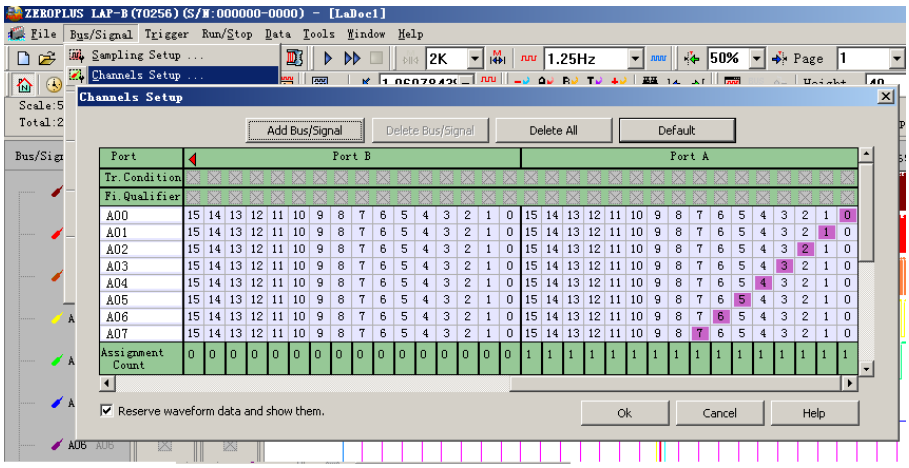


Fig 4-30 – Channels Setup

Rename the Bus and set up the channels of the Bus as shown in Fig 4-31.

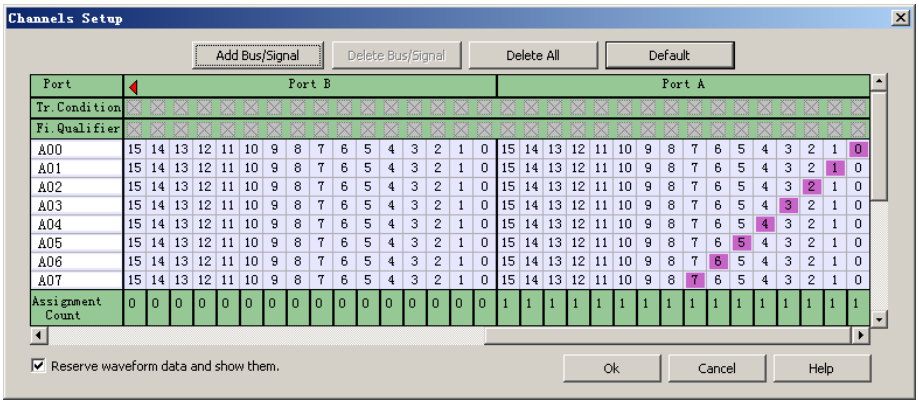


Fig 4-31 – Renaming Bus

1. Click the column with blue, type the given name of the Bus and then press **Enter** to confirm it.
2. Go to the relative channels as shown in Fig 4-31 and go to numbers 3, 4, 5, 6 which are located on column Port A and row Bus1. Click them to become purple, and then set these segments of signals.
3. Click **OK** to get the result as shown in Area 1.

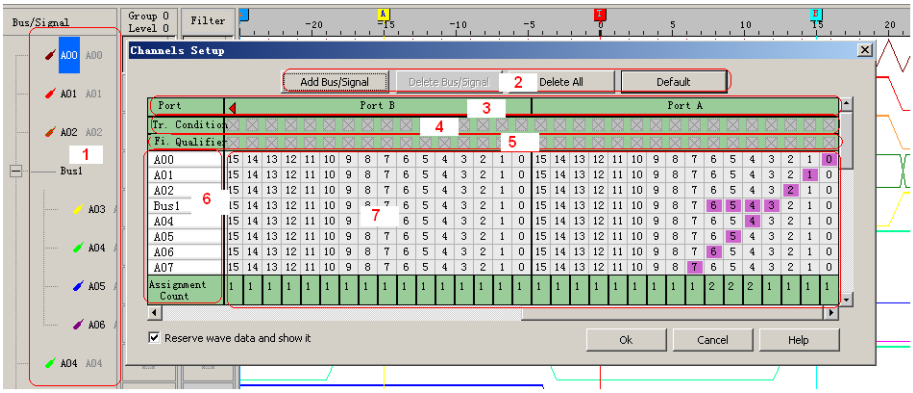


Fig 4-32 – Channels Setup Window

Tip: Channels Setup

In the dialog box of Channels Setup, there isn't only Add Bus/Signal, but also Delete Bus/Signal, Delete All, Default functions provided.

1. Delete Bus/Signal: Firstly highlight the Bus or channels on Area 6 of Fig 4-32, then click **Delete Bus/Signal** to delete it or them.
2. Delete All: Click **Delete All** to delete all Bus/signals on Area 6 of Fig 4-32.
3. Default: Click **Default** to restore the dialog box of Channels Setup as shown in Fig 4-30.

Step 3. Trigger Condition setup

1. Highlight the Bus which will be triggered, then click icon or select **Bus Trigger Setup** from the Trigger of the Menu Bar, the dialog box as shown in Fig. 4-33 will appear.

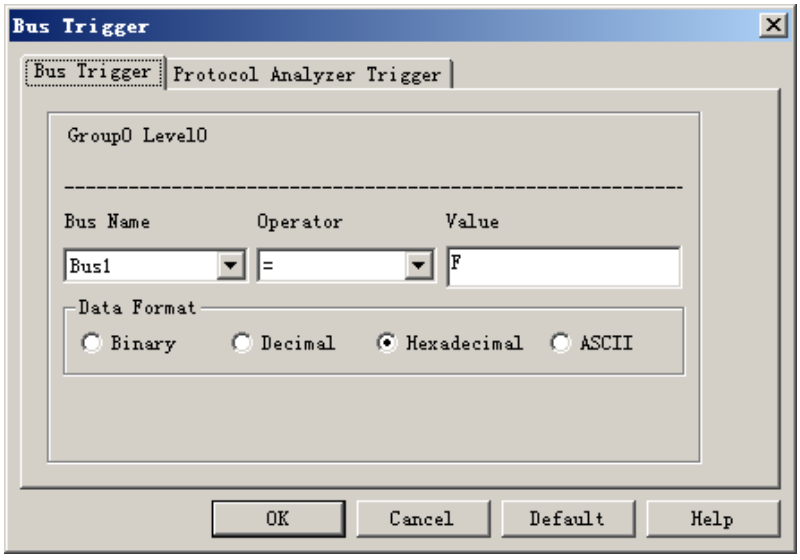


Fig 4-33 – Bus Trigger Setup

Tip: Double click on the trigger column of the Bus as shown in Fig 4-34.

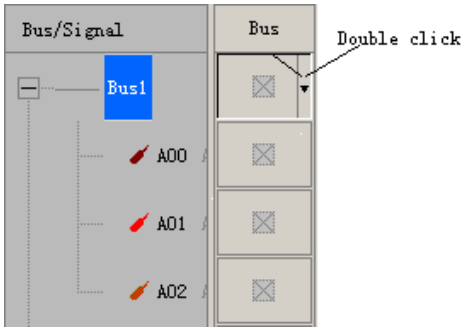


Fig 4-34 – Bus Trigger Column

2. Set Binary, Decimal，Hexadecimal or ASCII as the signal of the Bus to represent the value (see Fig 4-33).

3. Set " = " and type the value of Bus into Value column to set the trigger condition of the Bus.
4. Click **OK**.

Step 4. Click **Run** and activate the signal from the tested board to the system to get the result as shown in Fig 4-35.

Tip: Click icon to view all data, and then select the waveform analysis tools to analyze the waveforms.

Set Value is "3" as Hexadecimal, and set Operator equals to "= ", then click **OK.** Click **Run** and activate the signal from the tested board to the system to get the result as the trigger happens on 0X3.

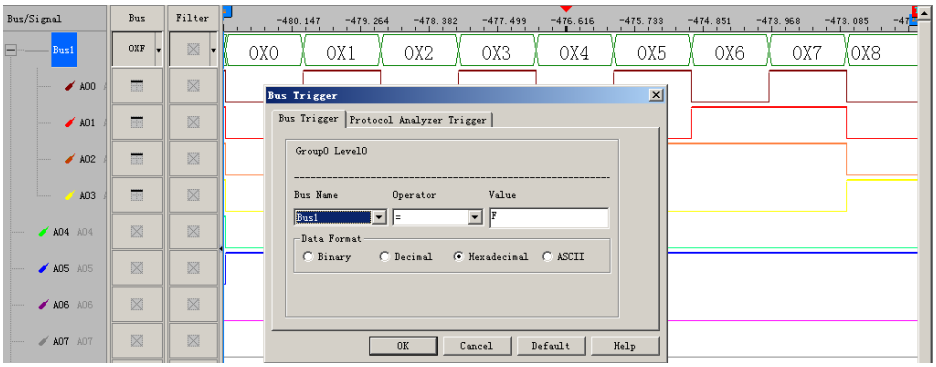


Fig 4-35 – Bus Trigger Setup

4.3 Plug Analysis

Plug Introduction

Protocol Analyzer operates in the form of plug; every Protocol Analyzer has a plug, and per plug is an independent modularization. One Protocol Analyzer plug can analyze many Buses at the same time, however, because the independence of every plug, the Protocol Analyzer plug only supports IIC, UART, SPI, HDQ, 1-WIRE, CAN2.0B at present. In the future, it will support more Protocol Analyzers; and when the Protocol Analyzer is renewed, it only need to download the new Protocol Analyzer plug and cover the old Protocol Analyzer plug; the speed is very fast.

Operating Instructions: There are PlugIns data file in the position of installing LA software. All Protocol Analyzer plugs which are used at present are put in the data file; the .DLL file can be added or deleted in the content, and in the Bus Property, all Protocol Analyzer plugs that can be used at present can be seen as the figure below:

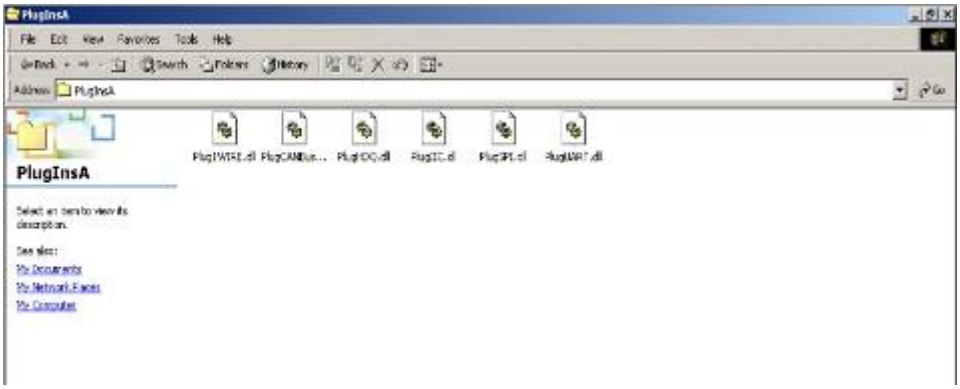


Fig4-36 - PlugInsA

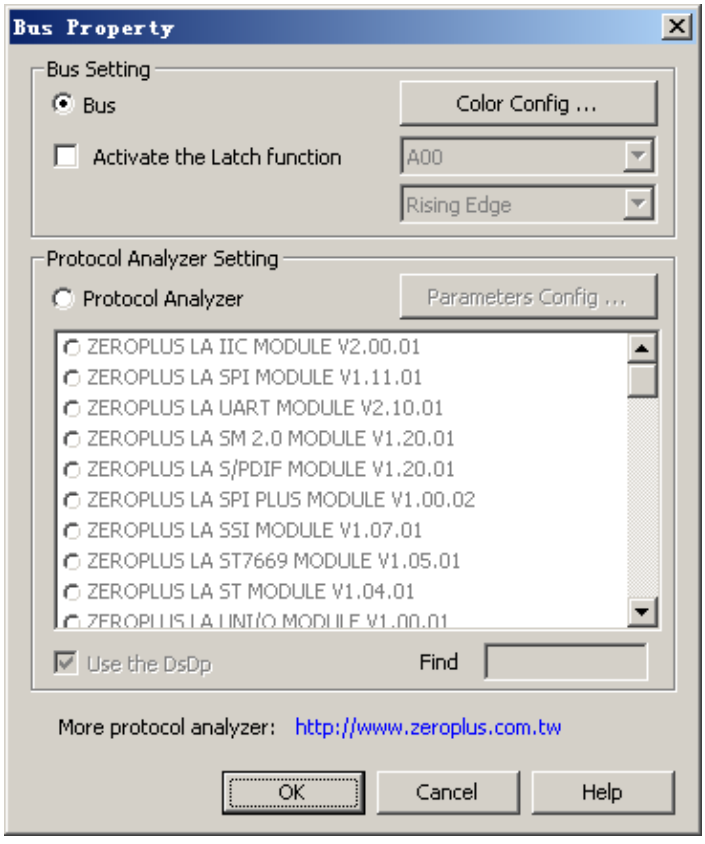


Fig4-37 - Bus Property

Every Logic Analyzer module supports some basic Protocol Analyzer plugs, however, when users need to use CCIR656 analysis, they can purchase it from our company, and then, they can get Protocol Analyzer CCIR656 plug and the register code.

STEP 1. Put the CCIR656 plug in the PlugInsA as the Fig4-38.

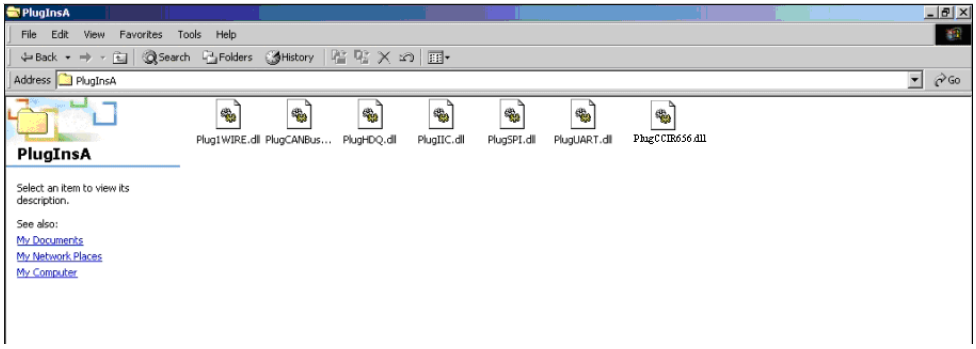


Fig4-38 - PlugInsA

STEP 2.Select CCIR656 in the list of Bus Property.

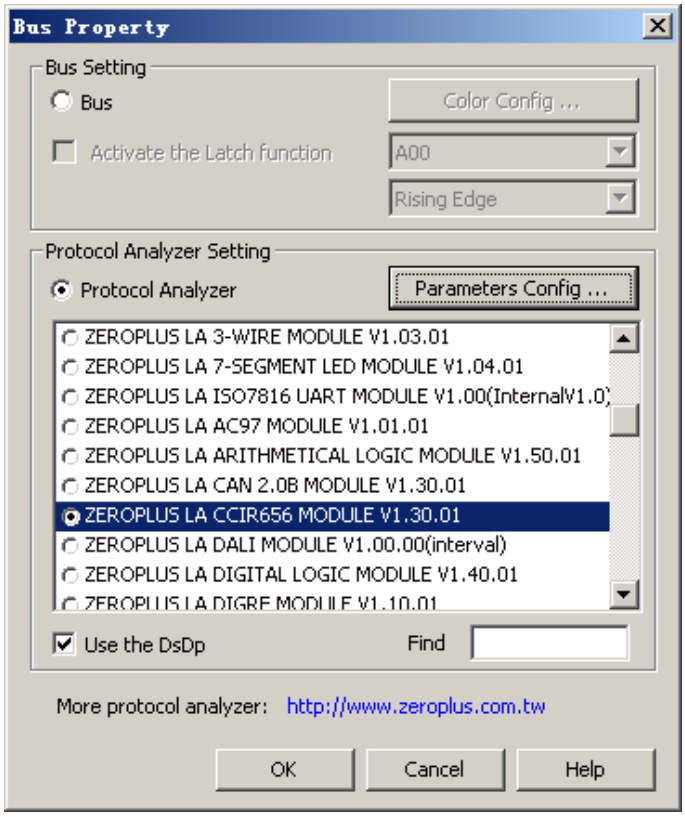


Fig4-39 - Bus Property

STEP 3.Click **Parameters Configuration** button, select Register dialog box and enter the serial key to use the Protocol Analyzer CCIR656.

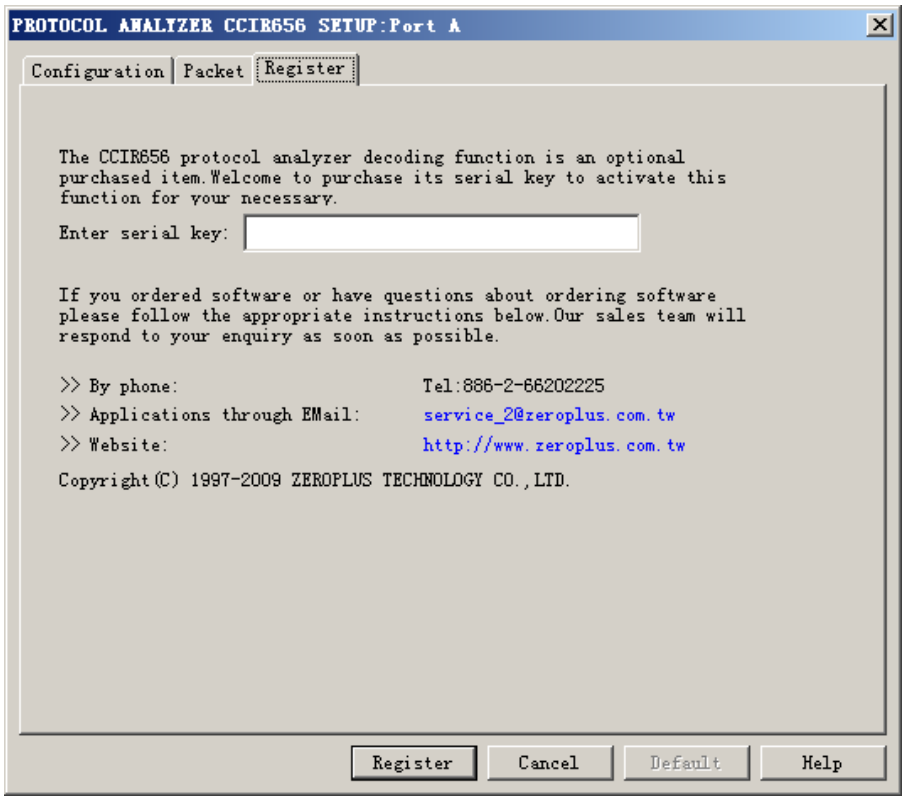


Fig4-40 - Protocol Analyzer CCIR656 Setup

4.4 Bus Packet List

Bus Packet List is a graphic list which is used for doing Statistic and showing Bus packet. It is visual and direct, especially for IIC, USB, CAN2.0B. When there is a packet list, it gets twice the result with half the effort to check the data. The Packet List has its startup button in the Tool Bar. After starting it, it will show a small window underside the waveform window. You can alter its size in order to find more data.

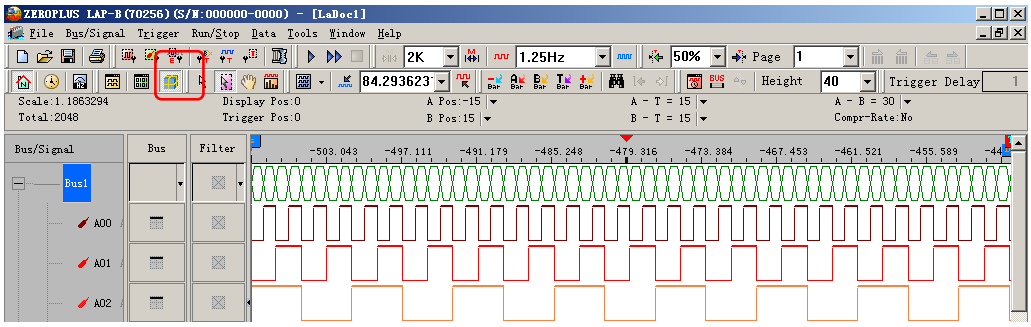


Fig 4-41 – Packet Startup

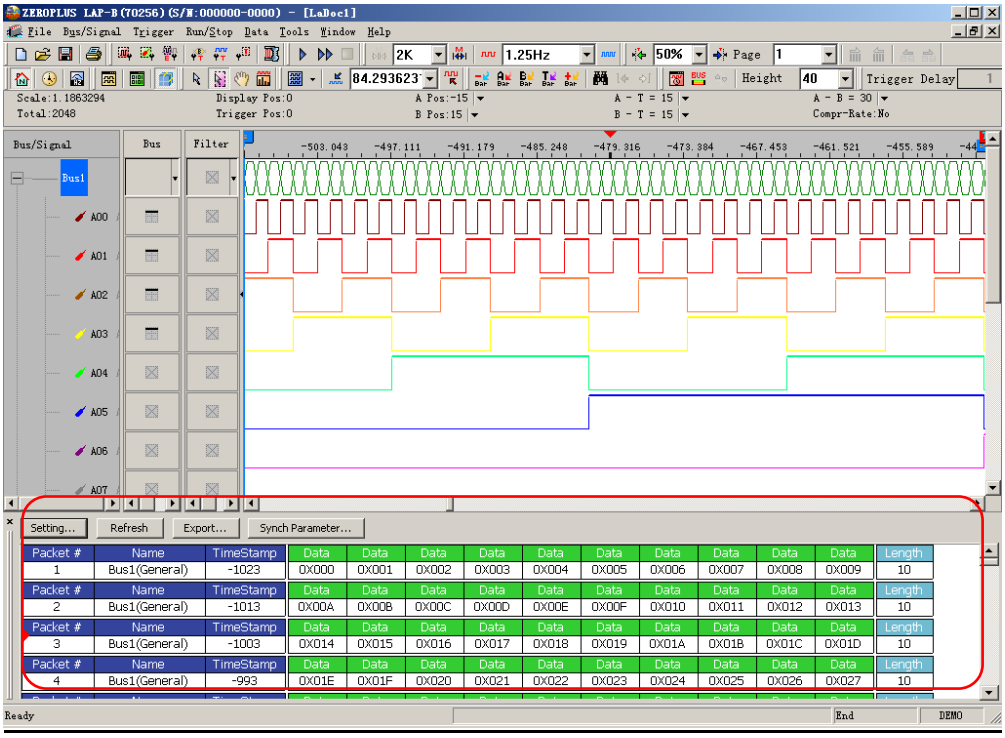


Fig 4-42 - Bus Packet List

The Packet List has setup windows; users can set up the parameters according to their requirements. Setting Bus Packet Length in the following dialog box is only used for doing Bus Statistic. Users can define how long the time is as a data packet in order to add the export function.

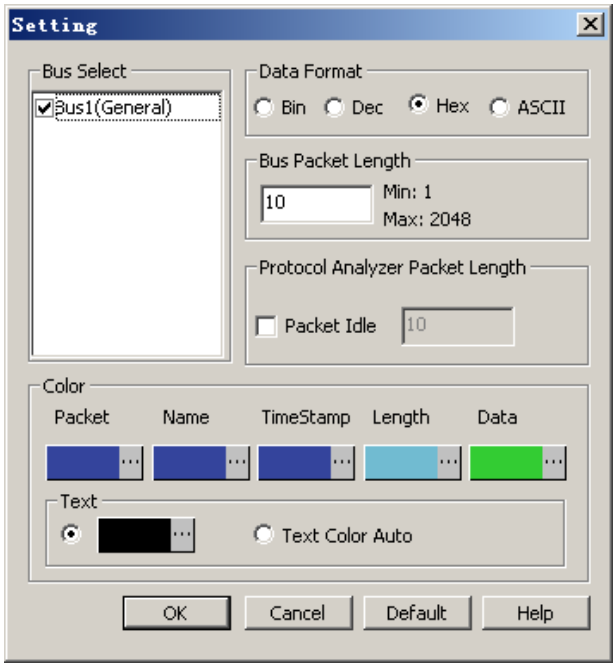


Fig 4-43 - Setting

Tip:

Customize Protocol Analyzer Packet Length

When Packet List deals with data packets of those modules which are in single data unit, however, this Packet is not convenient for users to observe, we need to add a function of customizing Packet Idle which allows users to input an idle time as users' requirements. When the packet is displayed, the program will decide which data should be put in the same packet according to the input time. And users can observe the packet better as a result of the customized idle time.

Add a customized packet idle time to the Bus Packet List Setting dialog box (see Fig4-43).

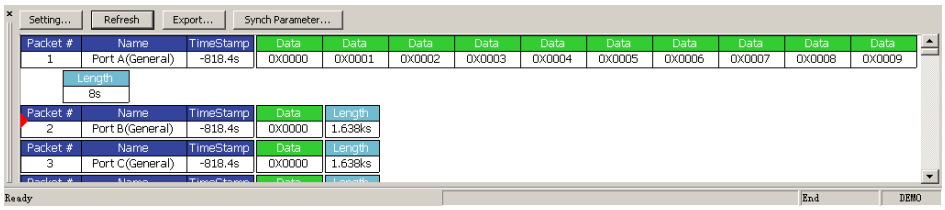


Fig 4-44 - General Bus Packet List

1. View Specifications

Packet#, Name and TimeStamp are the fixed items.

Packet#: Display the order of the packet.

Name: The name of the packet, or Signal Filter Display Bar.

TimeStamp: It is the start position of the packet.

Tip: The rest name and content are supplied by Plug.

Fig4-45 - Protocol Analyzer IIC Packet List

Setting: It is used to open Packet List Setting dialog box.

Refresh: Press this button, then the List View can renew automatically.

Export: Export files into Text (*.txt) and CSV Files (*.csv).

Synch Parameter: The data of the waveform is corresponding with the data of the packet list. Users move the waveform or the packet list, another will automatically move the corresponding data at the same time.

2. Display every Protocol Analyzer Packet in order.

Tip: The below view is Protocol Analyzer IIC whose packets are decided by the address of TimeStamp.

Fig4-46 - TimeStamp

TIP: When the Display Bar function of Signal Filter is activated, the Signal Filter Display Bar will be displayed in the Bus Packet List View as well as the TimeStamp, Address and Length of the Display Bar.

3. Packet Idle and Packet Length

Packet Idle: Packet Interval Time Packet Length: Packet Time Length

When those above two items are to be displayed, it only chooses one of them to display, which is controlled by Plug.

Because it is impossible that every Protocol Analyzer packet has registered TimeStamp and end, we add two special Unkonw_Flag to judge the TimeStamp and end of the packet; they are Unknow _Start_Flag and Unknow_End_Flag.

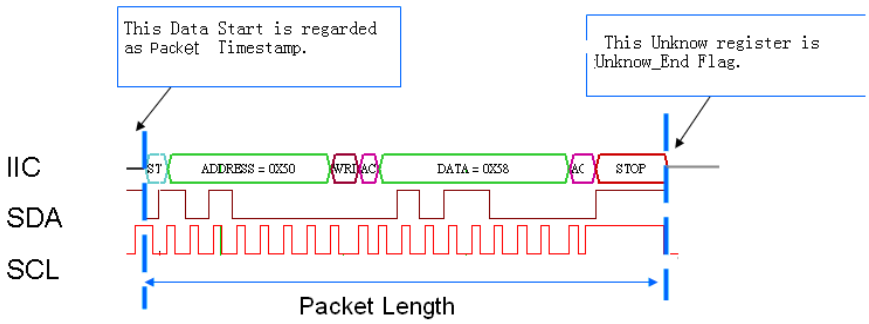


Fig4-47 - Protocol Analyzer IIC Packet Length

Tip: Because IIC has Start as the Packet Start, it needs not to use Unknow_Start_Flag as the TimeStamp.

4. Bus

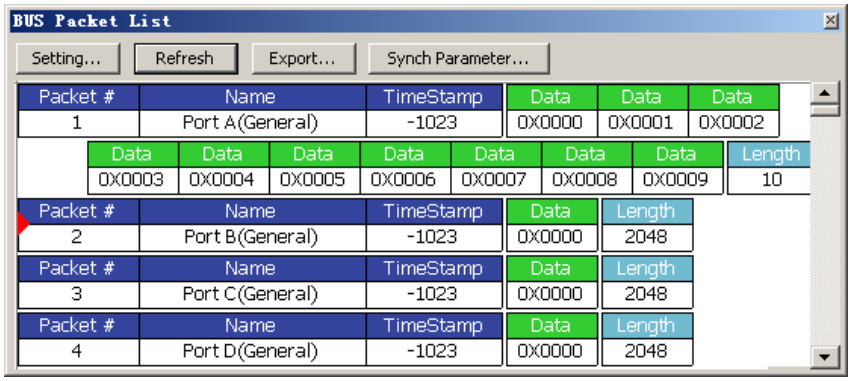


Fig4-48 - BUS Packet List

Packet Length and Packet Idle Length

Packet's Start is the start of Bus Data; the default length is controlled by the Setting dialog box. If the input packet length isn't the end of data, the software will prolong the length of the packet to end the data automatically as the figure below.

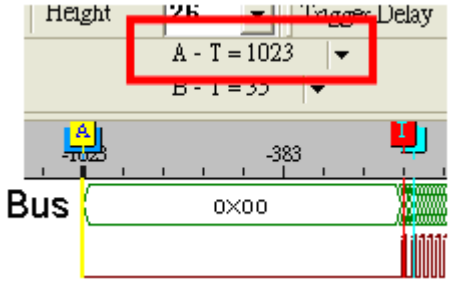


Fig4-49 - Auto-Prolong Packet

The Fig4-49 is a Bus; its first data is 0x00, and its length is 1023 addresses. If users input 20 addresses as the Bus Length. But 20 addresses is not the end of this data, then the software will prolong the length of the Packet to 1023 automatically.

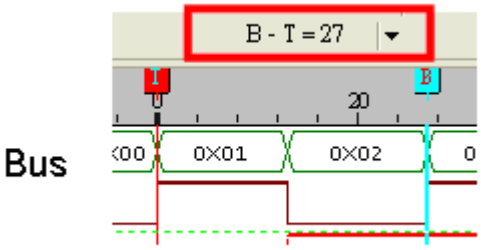


Fig4-50 - Packet End

The Fig4-50 is a Bus; if the start of the packet is T Bar, but the set Bus Length is 20 addresses, and the data 0x02 isn't the end; at that time, the packet will prolong to the end position automatically, that is to say, the Address 27 (B Bar) is the packet end.

The above two data are made consecutively as the figure below.

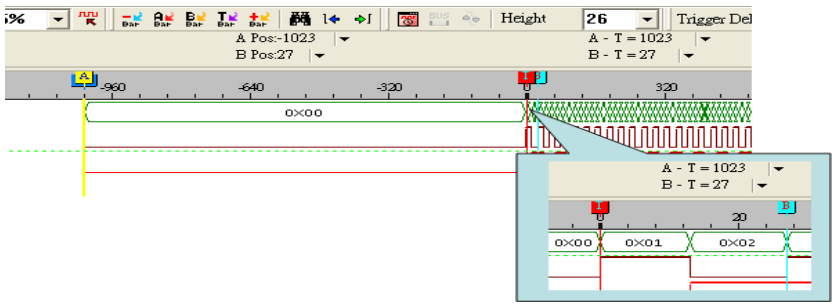


Fig4-51 - Auto-Prolong Packet

The Packet List is displayed as the figure below:

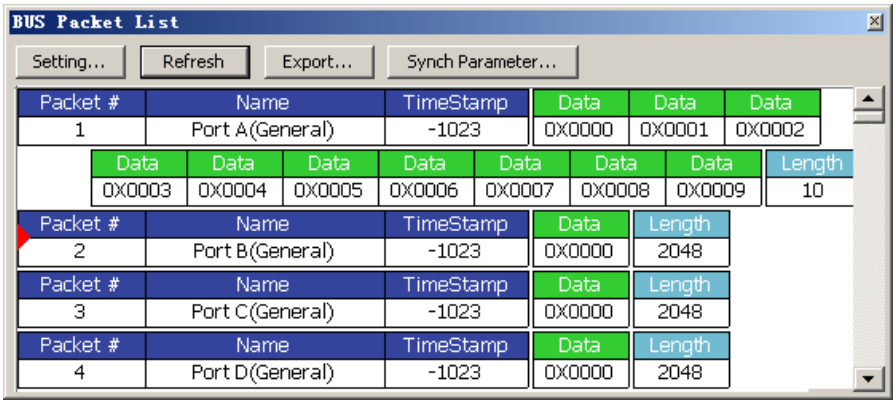


Fig4-52 - Bus Packet List

Tip: The Protocol Analyzer Packet will be explained in the following plug.

5. Packet and Waveform Synchronization

For the convenience of fast corresponding between packet data and waveform data, what is more, in order to make it easier for users to observe the data, we add the packet and waveform synchronization function.

In order to operate conveniently, we add a "**Synch Parameter**" button on the BUS Packet List as the image below:

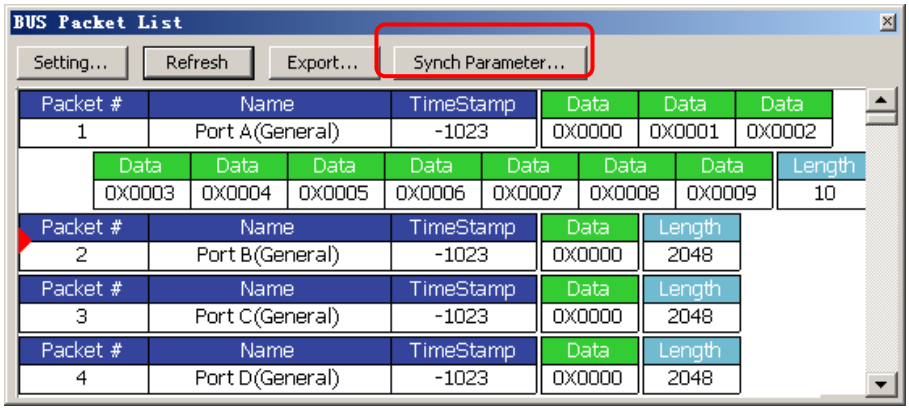


Fig 4-53 - Synch Parameter Setting

At the same time, a packet and waveform synchronization setting dialog box is added.

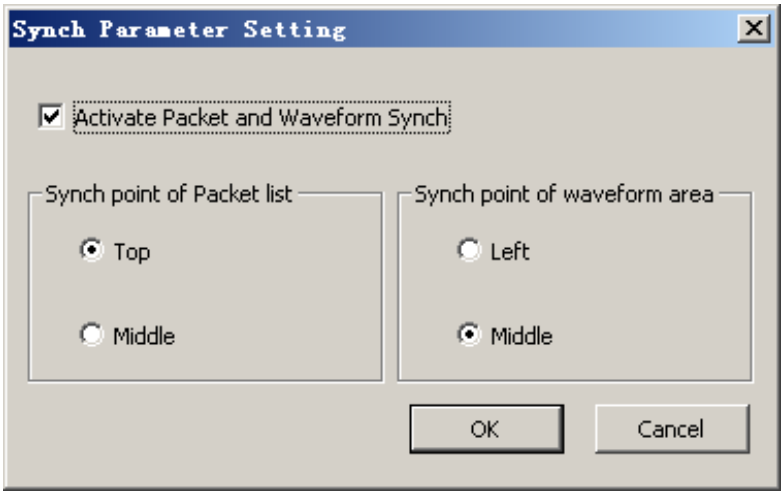


Fig 4-54 - Synch Parameter Setting Dialog Box

Activate Packet and Wave form Synch: The default is not activated.

Top: When Packet and waveform Synch is activated, the synch point in the packet list is the top packet segment which is displayed by list.

Middle: When Packet and waveform Synch is activated, the synch point in the packet list is the middle Packet segment which is displayed by list.

Left: When Packet and waveform Synch is activated, the synch point in the waveform area is the left packet segment which is displayed by waveform.

Middle: When Packet and Waveform Synch is activated, the synch point in the waveform area is the middle packet segment which is displayed by waveform.

Activate Packet and waveform Synch, and then select **Top** and **Left**.

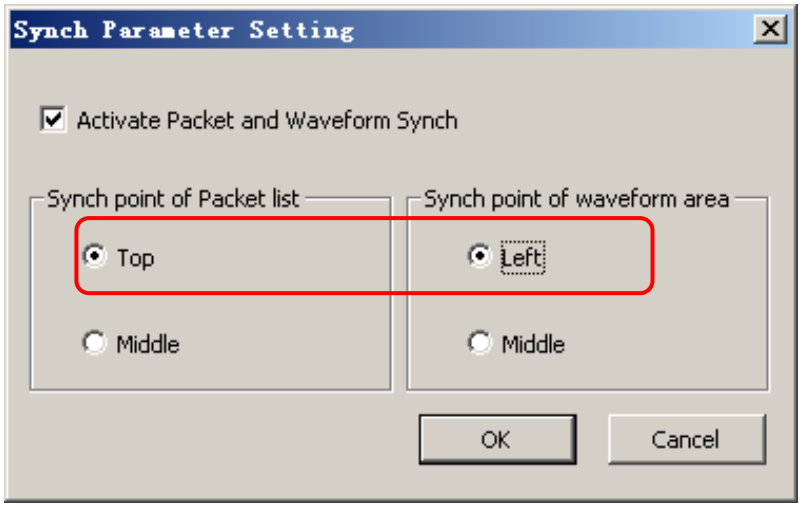


Fig 4-55 - Synch Parameter Setting Dialog Box

Display the corresponding of waveform and packet as below image:

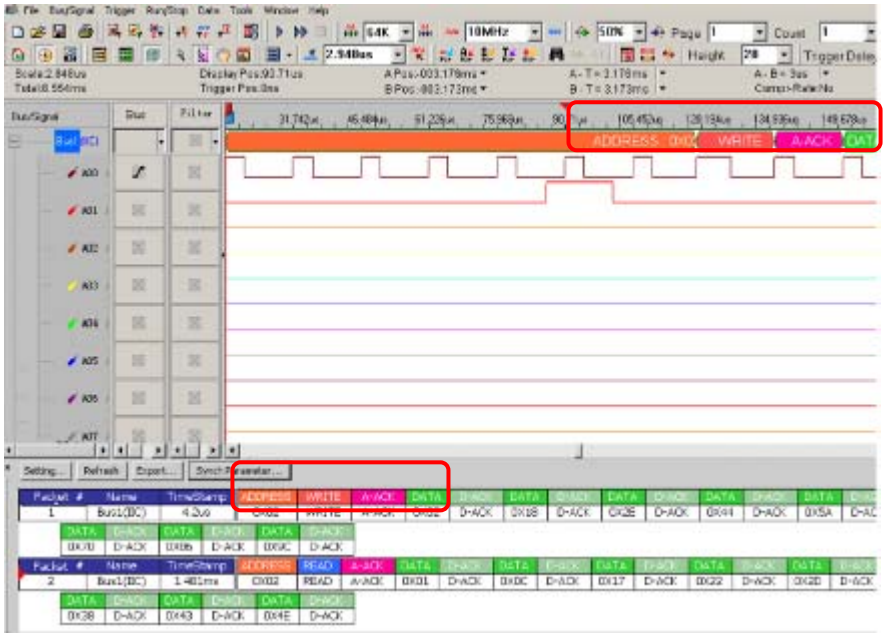


Fig 4-56 - Waveform and Packet Synchronization Interface

4.5 Bus Analysis

The setup is correlated to the Bus which needs to be made up, for example, Bus, Protocol Analyzer.

Open the dialog box:

STEP 1. Click **Tools** on Menu Bar, and then select **Bus Property** or select to set up Bus Property.

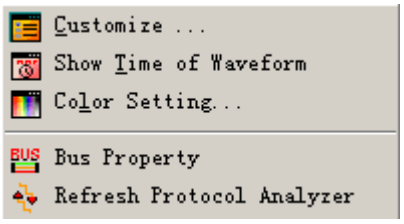


Fig4-57 - Set Bus Property

Fig4-58 - Bus Property

STEP 2. Click the right-key on the Bus/Signal column, and then select **Bus Property**.

Tip: The signal must be grouped into Bus, or the Bus Property cannot have effect.

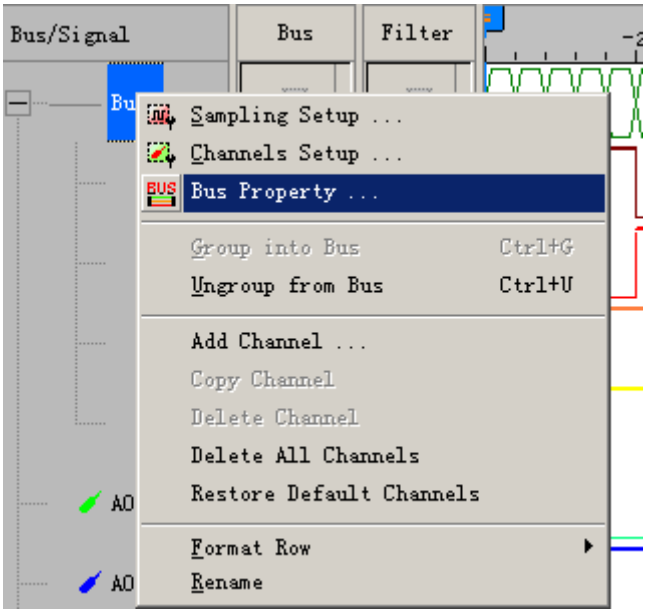


Fig4-59 – Click Right-key to Set Bus Property

4.5.1 Bus Analysis

The Bus function can make the system analyze Bus.

1. Basic Setup for the Bus

STEP 1. Click **Bus Property**, the following dialog Box will appear.

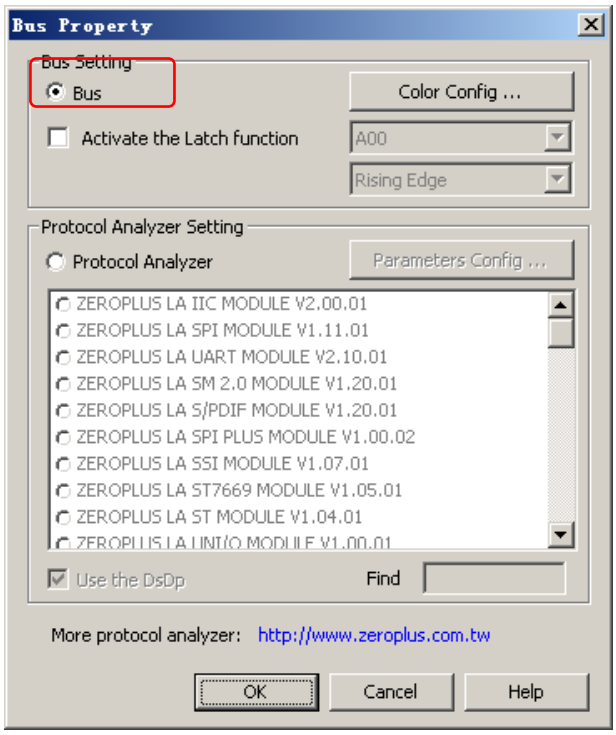


Fig4-60 - Bus Setting

STEP 2. Click **Color Configuration** to set Bus Data Color.

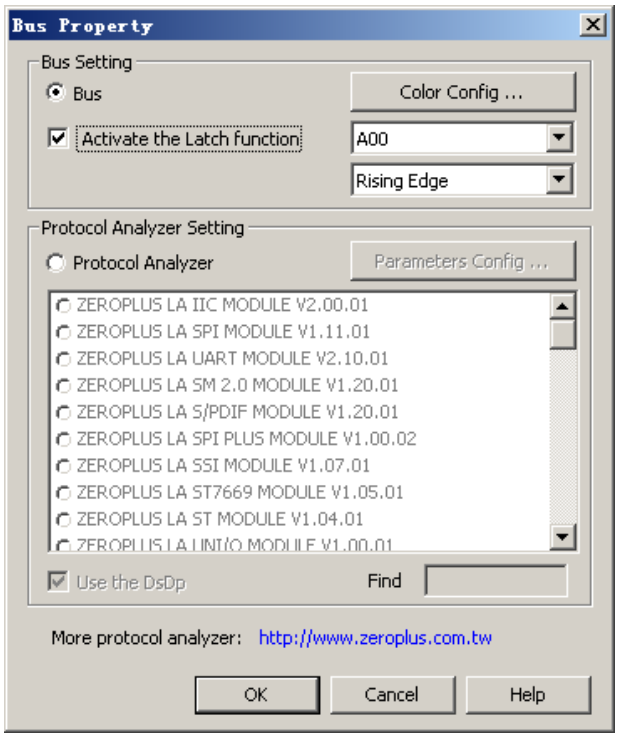


Fig4-61 - Color Configuration

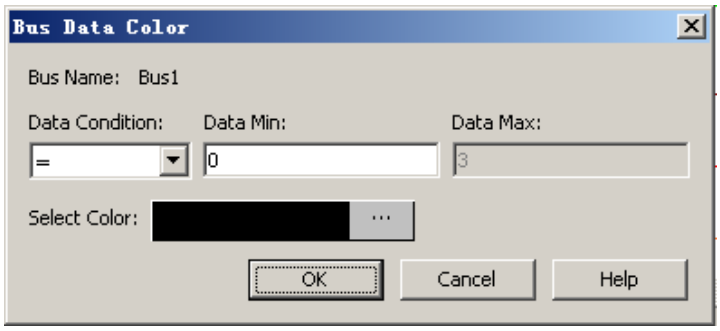


Fig4-62 - Bus Data Color

Bus Name: Display the selected Bus name.

Data Condition: Select the Data Condition to change the Bus data color. There are four options which are =, !=, In Range and Not In Range.

Data Min.: Enter the min. data that is required by users.

Data Max.: Enter the max. data that is required by users. The max. data can be used only when the data condition is set in range.

Select Color: Select the changed color according with the data condition which is set by users.

STEP 3. Set the color of the Bus. Data =5 whose color is Orange.

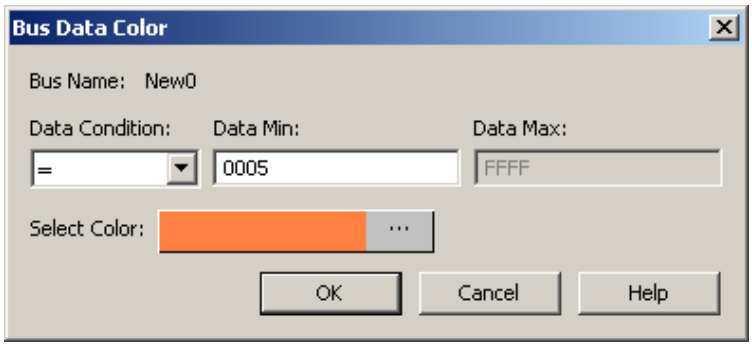


Fig4-63 - Set the color for New0.

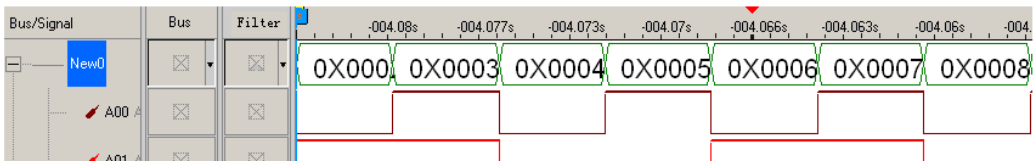


Fig4-64 – Before the Bus Data Color Setting

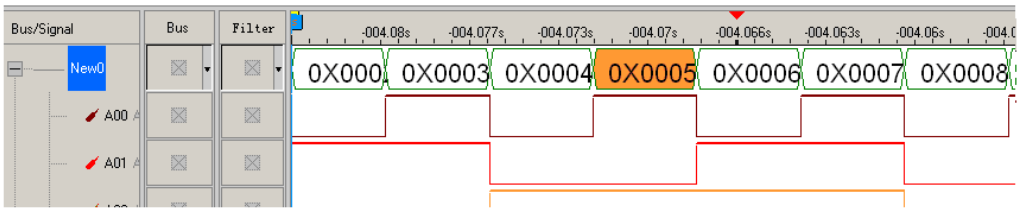


Fig4-65 - After the Bus Data Color Setting

Tips: 1. Set the conditions of the Color Configuration in the General Bus Setting, and carry out the operation of Run.

The color of the data set in the Bus Data Color dialog box won't be deleted, and the set color is still

displayed on the waveform area after Run.

2. Reserve the original state by the above steps.

STEP 4. Activate the Latch function

Activate the Latch function: The default is not activated. When the Latch function is activated, the default channel is A00, and there are three conditions for selecting, Rising Edge, Falling Edge and Either Edge; the default is Rising Edge.

Set the Latch function for one Bus. The set Latch channel is A00; the analysis condition is set as Rising Edge.

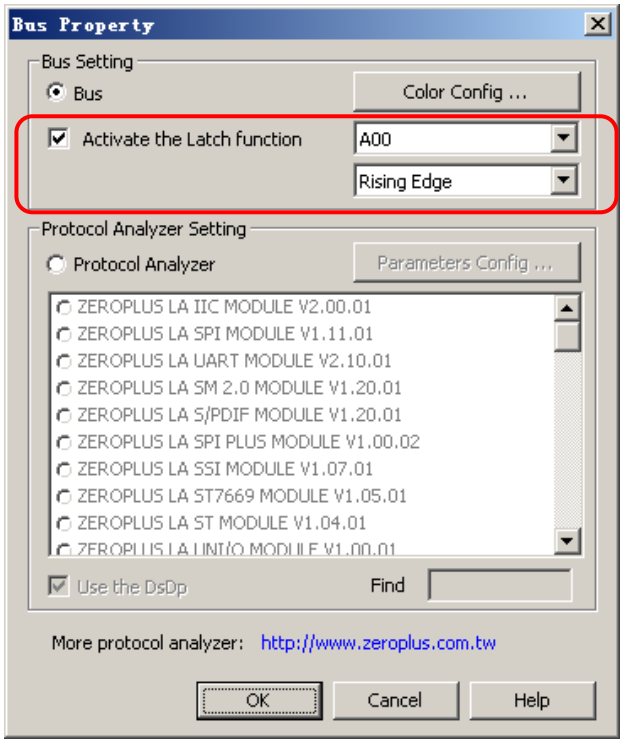


Fig4-66 - Activate the Latch Function

The picture of the waveform analysis:

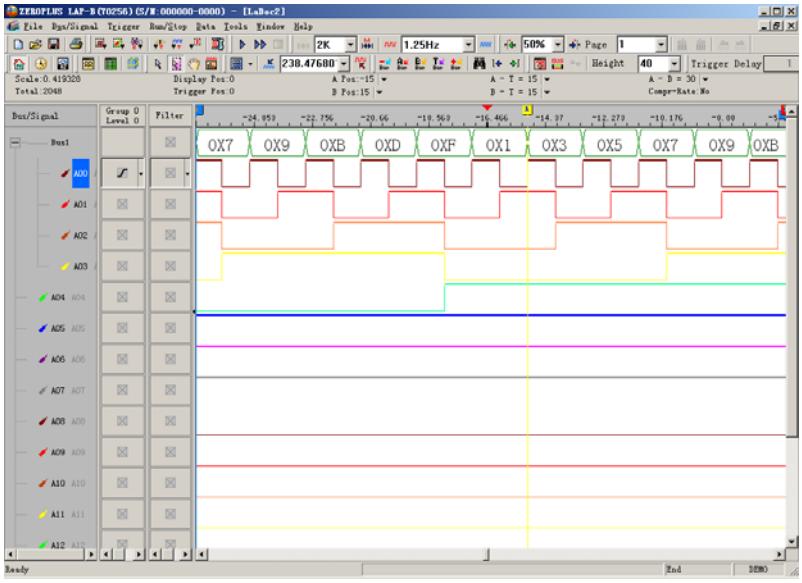


Fig4-67 - The Latch Function Displayed on the Waveform Area

Illustration: The selected channel is A00; the analysis mode is Rising Edge; it indicates that the data of A00 is read

at the Rising Edge. See the A Bar in the above figure, the data of Bus1is 0X1.

2. Protocol Analyzer Setting

In this version, there are six analyses about Protocol Analyzer which are IIC, UART, SPI, 1-WIRE, HDQ and CAN2.0B. They are detailed illustrated in the following six sections.

4.5.2 IIC Analysis

IIC Introduction

The IIC, which stands for Inter-Integrated Circuits, is a serial synchronous half-duplex communication protocol. The IIC was first proposed by Philips Semiconductor Netherlands. This IIC protocol consists of a very simple physical interface which has only two signal channels, SDA (Serial Data) and SCL (Serial Clock). Most IIC devices consist of an independently sealed IIC chip, and this IIC chip has direct connection to both SDA and SCL. The data transmission is a byte-base (8-bit base) for every segment. Since many oscilloscopes do not allow engineers observe timing sequence information directly from the screens of oscilloscopes, this Logic Analyzer was created to help engineers resolve timing sequence issues during their circuit development.

IIC has a multi-control Bus as its physical and firmware interfaces. This Protocol Analyzer is basically a signal network that may connect to one or several control units. The intention of inventing this protocol was in the application of designing television sets, which allowed the central processing unit to quicken data communications with peripheral chips and devices. The IIC interface is initiated with a SDA triggered **High** and SCL triggered **Falling Edge**. Following the initiation, there will be a set of 7 bits (or 10 bits) address space. Beyond this point, there will be Read/Write, ACK (Acknowledgement), and STOP (or HALT/HLT). The signal information packet is transmitted in bytes. If there are two or more devices trying to access the Protocol Analyzer IIC , whichever device has SCL at logic high will gain access priority.

Furthermore, since IIC is a synchronous communication protocol and data transmission must be in bytes, a complete IIC signal packet must consist of **START**, **ADDRESS**, **READ/WRITE**, **DATA**, **ACK/NACK**, and **STOP** segments. They are as following.

START: This is the initiation of SCL and SDA (1 bit only).
ADDRESS: This identifies the device address (7 bits).
READ/WRITE: This is a data direction bit. 0 = Write, 1 = Read.
ACK/NACK: This is a confirmation bit following every data transmission segment.
DATA: The actual signal data transmitted by byte.
STOP: This appears when SCL = High and SDA = Low (1bit only).

4.5.2.1 Software Basic Setup of Protocol Analyzer IIC

Step 1. Set up RAM Size, Frequency, Trigger Voltage and Trigger Position as described in Section 4.1.

Step 2. Set up the Falling Edge of the trigger condition on the signal which connects to the tested IIC data pin (SDA).

Step 3. Group the unanalyzed channels into Bus1.

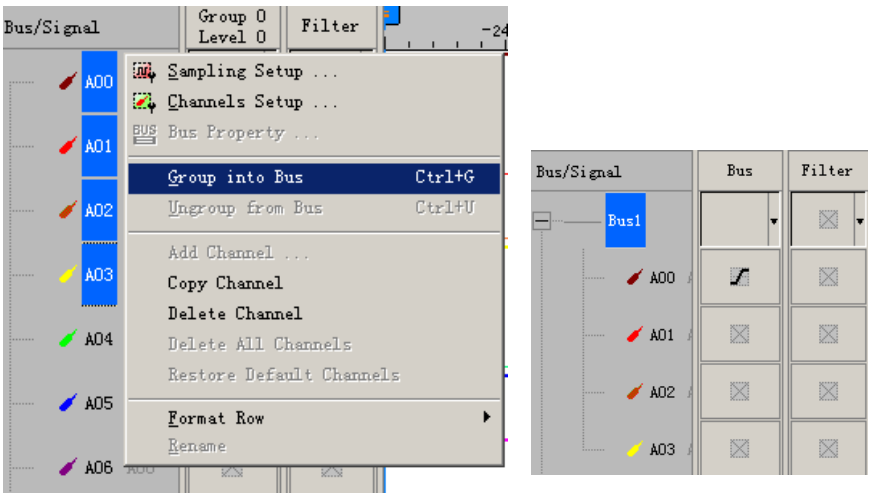


Fig4-68 - Group into Bus

Step 4. Select Bus1, then press the right-key on the mouse to list the menu. Next, click **Bus Property** or click **Tools** to select "Bus Property" or click

to open **Bus Property** dialog box.

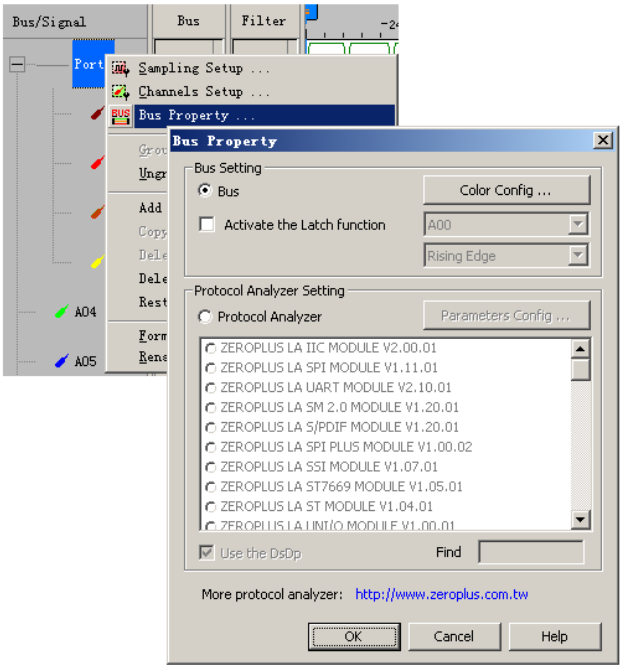


Fig4-69 - Bus Property

Step 5. For Protocol Analyzer Setting, select Protocol Analyzer. Then, choose ZEROPLUS LA IIC MODULE V2.00.01, click "Parameters Configuration".

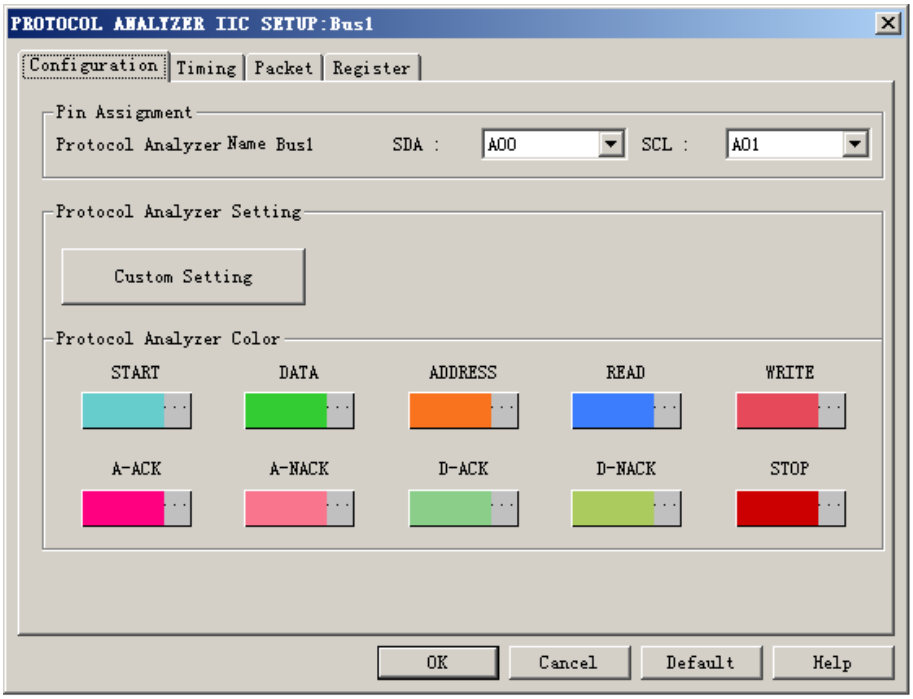


Fig 4-70 – Protocol Analyzer IIC Setup

Step 6. Set the **Pin Assignment**.

1. Pin Assignment: Set the display name of IIC in Bus1.
2. SDA: Choose SDA channel for IIC.
3. SCL: Choose SCL channel for IIC.

Note: It is recommended that SDA and SCL channels are named SDA and SCL to help distinguish between them.

4. Protocol Analyzer Color: Set the colors of the segment in Protocol Analyzer.

Step 7. Click **Custom Setting** to define the IIC Data to meet users' requirements. The dialog box as shown in Fig 4-72 will be displayed.

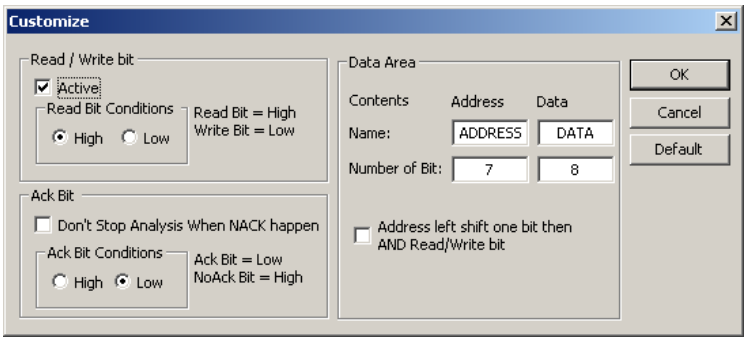


Fig 4-71 – Custom Setting

1. Read/ Write bit Setup:
   Click on "Active" to set the segment of **Read/ Write bit** in the Protocol Analyzer IIC , then select "High" or "Low" to set the active condition of the Read/ Write bit for the DUT.
   Click off "Active" to remove the Read/ Write bit segment from the IIC Data.
2. Ack Bit Setup:
   Click on "Don't Stop Analysis When NACK happen" to continuously analyze the signals when the system reads NACK bit, then select "High" or "Low" to set the active condition of the NACK bit for the tested Protocol Analyzer IIC .
   Click off "Don't Stop Analysis When NACK happen" to stop analyzing the signals when the system reads NACK bit.
3. Give the names and the numbers of bits to the Address bit and Data bit on the columns located in

Data area for the tested Protocol Analyzer IIC.
The range for "Number of Bit" is from 1 to 28 bits.

4. Click on "Address left shift one bit then AND Read/Write bit" to have an additional 1 bit on the right side of the Address Data content.
5. Press "OK" to confirm the setup of IIC Customize and return to the Protocol Analyzer IIC Setup dialog box. (**Tip:** Press **Default** to give up the current setup conditions)

Step 8. Press **OK** to exit the dialog box of Protocol Analyzer IIC Setup.

Step 9. Click **Run** to acquire IIC signal from the tested IIC circuit.

Tip: Click the IIC icon, then press **Stop** to exit IIC analysis mode.

Tip: Click icon to view all data, and then select the waveform analysis tools to analyze the waveforms.

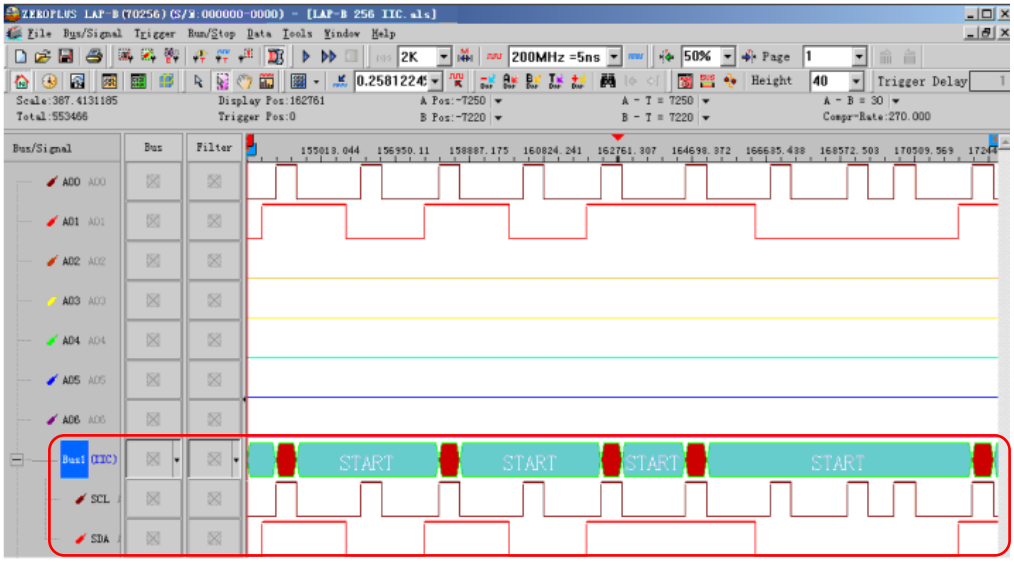


Fig 4-72 – Waveform Analysis

4.5.2.2 Protocol Analyzer IIC Timing Analysis

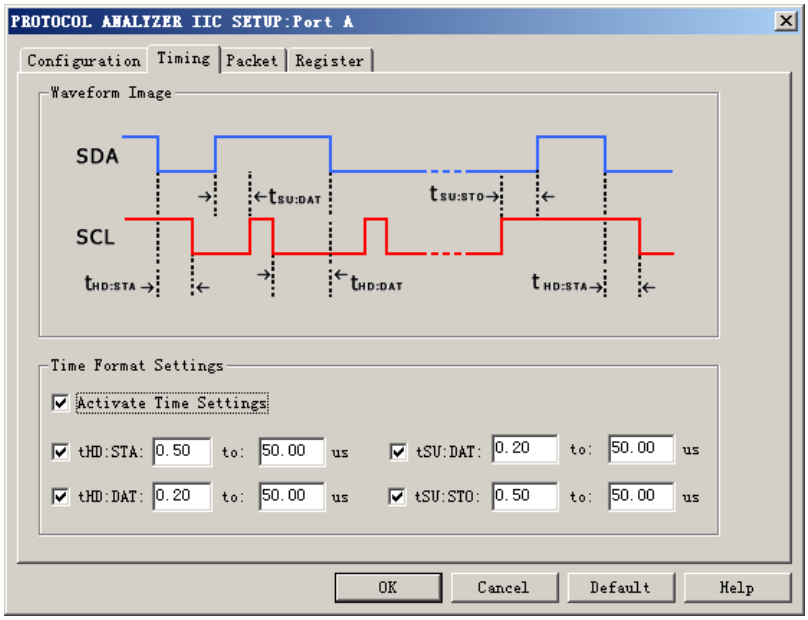


Fig-4-73 - Protocol Analyzer IIC Timing Setup

Waveform Image: Describe the position of the setting time.

Time Format Settings: When the Time Format Settings are activated, the set time will become the condition of judging decoding. For example, when you want to decode START, you should judge whether the conditions of START are satisfied firstly, and then judge whether the set time of tHD: STA is suitable for the factual waveform; if the two conditions are satisfied, the START could be decoded. The theory of START decoding is the same to that of other packet segments.

4.5.2.3 Protocol Analyzer IIC Packet Analysis

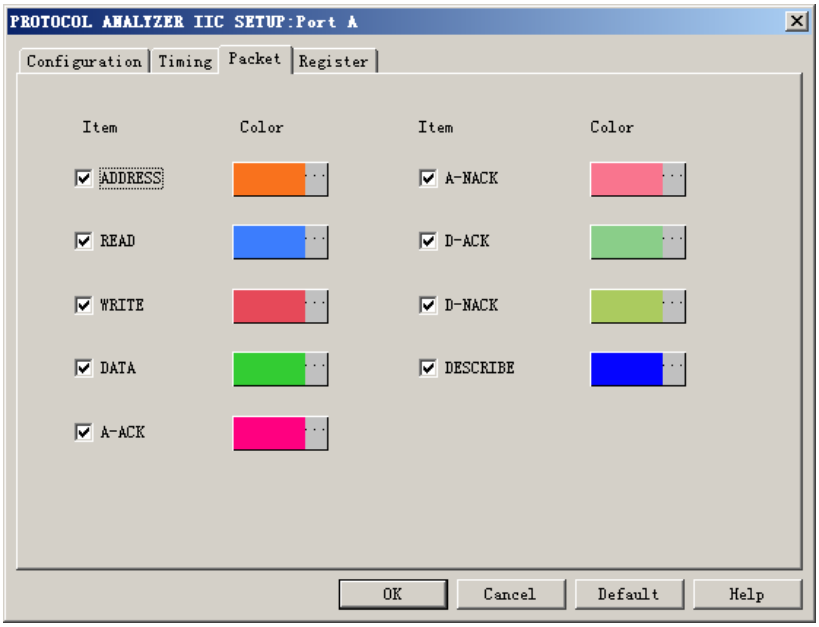


Fig4-74 - Protocol Analyzer IIC Packet

ADDRESS: Start bit address or Time display.

READ: Read field display in Packet.

WRITE: Write field display in packet.

A-ACK/A-NACK: A-ACK field has 2bits in all. If it receives success, it sends back "0", "1". If it isn't "0", "1", it displays "A-NACK".

DATA: List the data field captured signal by bus in Packet display.

D-ACK/D-NACK: It has 2bits. If it receives success, it sends back "0", "1". If it isn't "0", "1", it displays "D-NACK".

DESCRIBE: Error description to any field (format or data bit).

It is BUS Packet List View which includes 4 formats, which IIC happens as below.

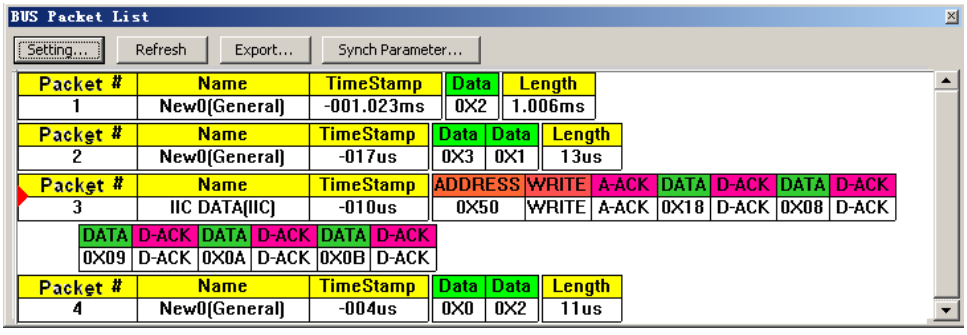


Fig4-75 - Protocol Analyzer IIC Packet List

Packet 1: It is commonly normal data which includes 1 "DATA".

Packet 2: It is commonly normal data which includes 2"DATA".

Packet 3: It is commonly normal data which includes 1 "ADDRESS" and 5 "DATA".

Packet 4: It is commonly normal data which includes 2"DATA".

Packet Length:

When judging to the start of IIC, it is the Packet TimeStamp.

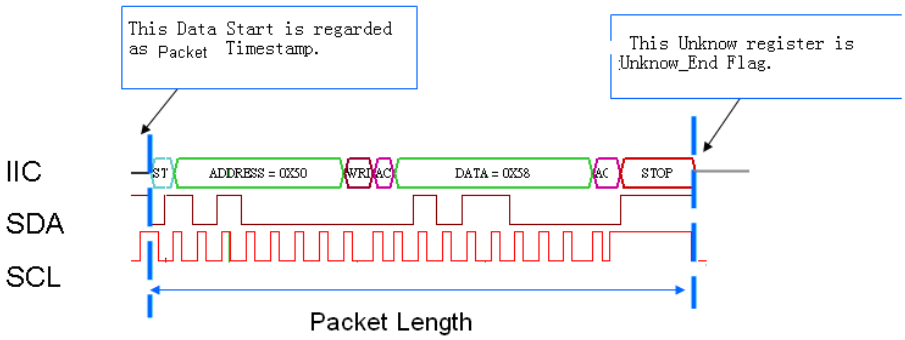


Fig4-76 - Packet Length

Packet Length: From Start's TimeStamp to Unknow_End Flag TimeStamp.

Packet Idling Length: From Unknow_End Flag TimeStamp to Start's TimeStamp.

This Unknow register is Unknow_End Flag.

4.5.3 UART Analysis

UART Introduction

The UART, which stands for Universal Asynchronous Receiver/Transmitter, is a serial asynchronous protocol. The UART is often time-integrated into PC communication devices, and it usually equips an EEPROM (Electronic Erasable/Programmable Read Only Memory) for error checking proposes with other chips. There are two concepts about UART which must be understood before performing any further tasks.

The UART protocol will first translate a parallel data into serial data, for the UART requiring only one wire to transmit signals. The transmission starts at a triggered Low position, and there are 7 or 8 bits of data following afterwards. To halt a transmission, it requires a signal or multiple bits of logic '1'. Odd number bit transmission requires odd parity error checking, and even number bit transmission requires even number error checking. Following the parity check is another data translation from serial data into parallel data. UART also generates an extra signal to indicate receiving and transmitting conditions.

Furthermore, since UART is an asynchronous communication protocol and data transmission may not be in bytes, a complete UART signal packet must consist of **START**, **DATA, PARITY**, **STOP, Baud** and **TXD** segments. They are as following：

START:	When TXD is changing from **HIGH** to **LOW** voltage (1 bit).
DATA:	Users must decide the size of signal packet segment from 4 to 8bits.
PARITY:	This performs three types of parity checks: odd parity, even parity, and none parity.
STOP:	This occurs when TXD is at high voltage. This is adjustable; this is commonly set to 1 or 2.
Baud:	This is the data transmission speed according to the initial condition of START.
TXD:	This is the transmission direction. It is MSB ➔ LSM by default.

4.5.3.1 Software Basic Setup of Protocol Analyzer UART

Step 1. Set up RAM Size, Frequency, Trigger Voltage and Trigger Position as described in Section 4.1. (Tip: The Setup of the Frequency should be higher, but not too far away from the Baud Rate of the tested board).

Step 2. Set up Either Edge as the trigger condition on the signals which are connected to the Tx pin or the Rx pin of the tested UART board.

Step 3. Set up the Protocol Analyzer Dialog Box which is set as the steps of IIC.

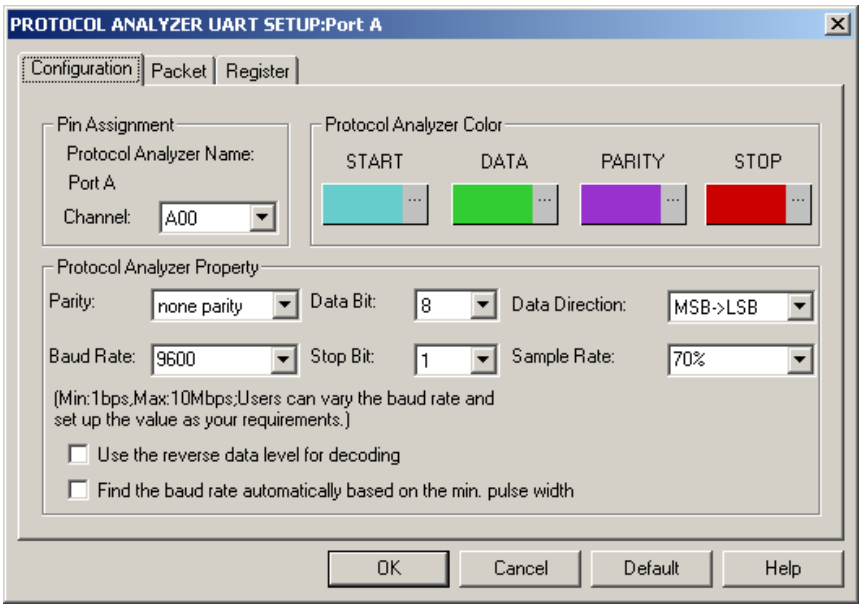


Fig 4-77 – UART Setup

Step 4. Protocol Analyzer UART Setup

1.Set the Data of the Transmitter Signal.

Select Pin Assignment, then choose the given Protocol Analyzer name for Port A. Next select the signal which is connected to the pin of Port A of the tested board from the pull-down menu to analyze the data of the transmitter signal.

2.Set the Baud Rate.

Select the baud rate from the pull-down menu of the Baud Rate to meet the specification of the tested UART board. Baud Rate can be set and equal to 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600 or 115200.

3. Set the bits for the Data Bit.

Select the number from the pull-down menu of the Data Bit to meet the specification of the tested UART board. Data Bit can be set as 4, 5, 6, 7 or 8.

4. Set the Data Direction.

Select MSB -> LSB or LSB -> MSB from the pull-down menu of the Data Direction to meet the specifications of the tested UART board.

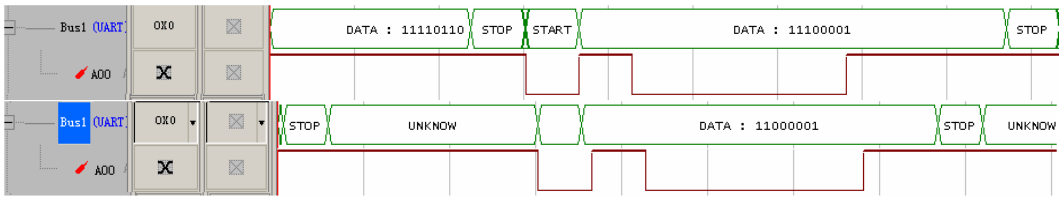


Fig 4-78 – Data Waveforms about MSB ->LSB and LSB ->MSB

5. Set the Parity
   Select "none parity", "odd parity" or "even parity" from the pull-down menu of the Parity to meet the specifications of the tested UART board.

6. Set the bits for the Stop Bit.
   Select the number from the pull-down menu of the Stop Bit to meet the specifications of the UART DUT. Stop Bit can be set as 1, 1.5 or 2.

7. Set "Use the reverse data level for decoding".
   Click on "Use the reverse data level for decoding" to decode the received data into the negative logic which a negative voltage represents the 1 state and which a positive voltage represents the 0 state.

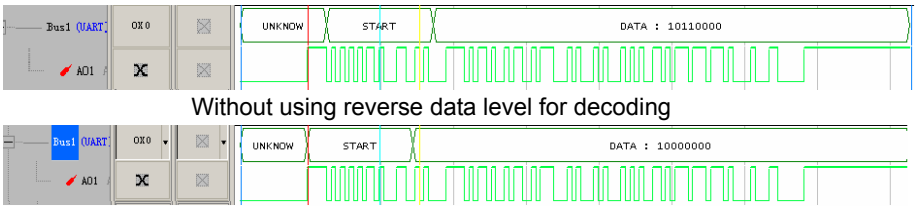


Fig 4-79– Without/With reverse data level for decoding

8. "Find the baud rate automatically based on the min. pulse width".

   Select **Find the baud rate automatically based on the min. pulse width** to find the baud rate automatically.

9. Set Protocol Analyzer Color
   Click the color of the packet segments as the DATA, the START, the STOP, and the PARITY to select the required color.

Step 5. Press **OK** to exit the dialog box of Protocol Analyzer UART Setup.

Step 6. Click **Run** to acquire the UART signal from the tested UART circuit.

Tip: Click icon to view all data, and then select the waveform analysis tools to analyze the waveforms.

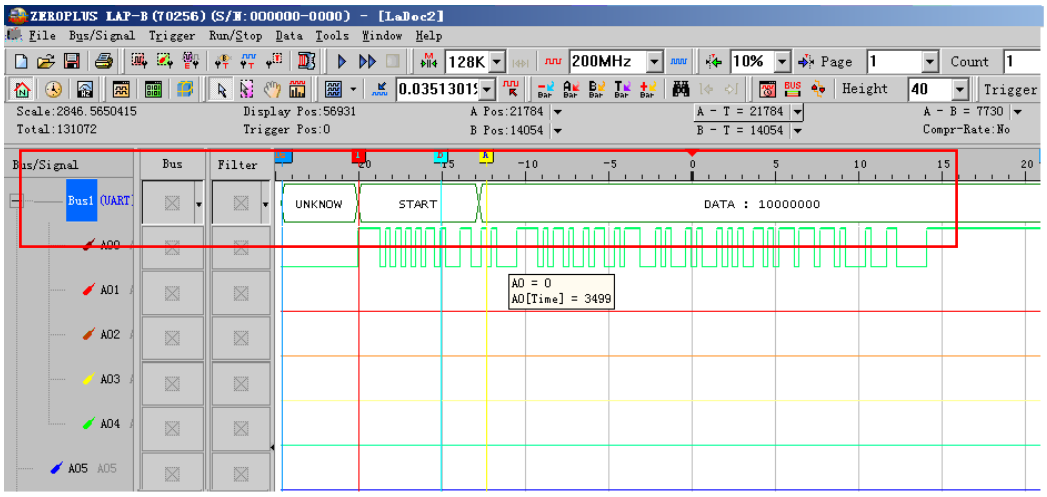


Fig 4-80 – Waveform Analysis

4.5.3.2 Protocol Analyzer UART Packet Analysis

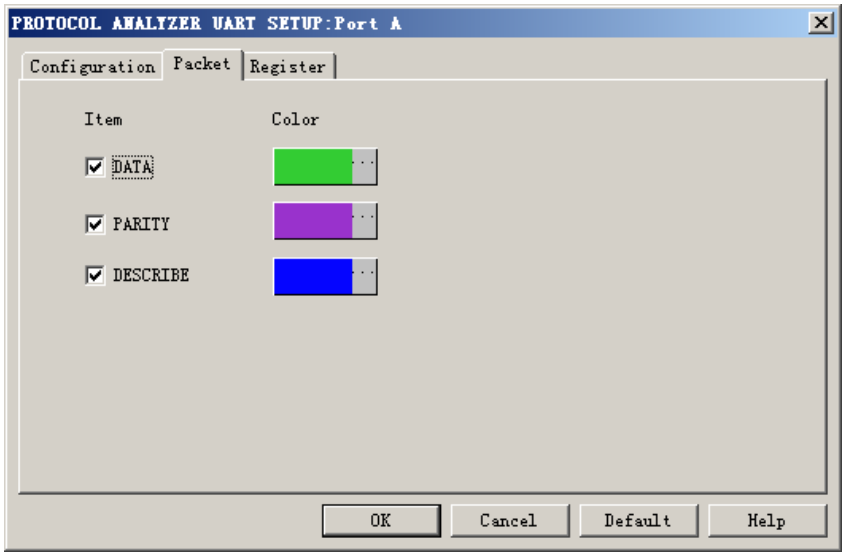


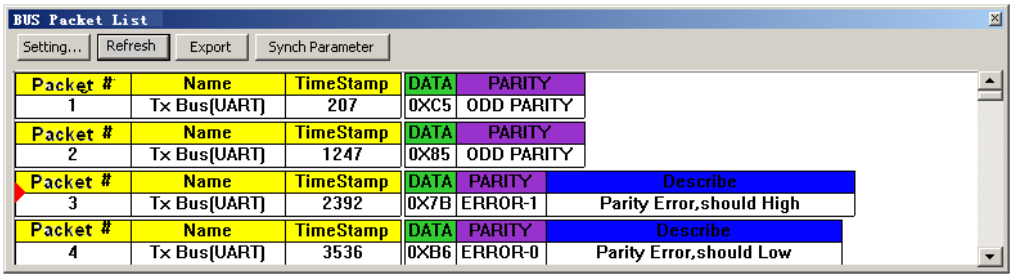
Fig4-81 – Protocol Analyzer UART Packet

DATA: List Data field captured by Bus in the packet display.

PARITY: Display parity check in the packet.

DESCRIBE: Error description to any field (format or data bit).

It is BUS Packet List View which includes 4 formats, which UART happens below. PARITY clews whether users start PARITY or not.



Packet #	Name	TimeStamp	DATA	PARITY	Describe
1	Tx Bus(UART)	207	0XC5	ODD PARITY	
2	Tx Bus(UART)	1247	0X85	ODD PARITY	
3	Tx Bus(UART)	2392	0X7B	ERROR-1	Parity Error,should High
4	Tx Bus(UART)	3536	0XB6	ERROR-0	Parity Error,should Low

Fig4-82 - UART Packet List

Packet 1: It is commonly normal Data which includes 1 DATA and 1 PARITY; its parity is ODD.

Packet 2: It is commonly normal data which includes 1 DATA and 1 PARITY; its parity is ODD.

Packet 3: It is the state of PARITY ERROR; the Describe is "Parity Error, should High ".

Certainly, EVEN and ODD are impossible to present the same Protocol Analyzer; it is used for exhibition here. So EVEN and ODD cannot appear at the same time.

Packet 4: It is the state of PARTIY ERROR; the Describe is "Parity Error, should Low".

Packet Length: When judging the START of UART, it is the Packet TimeStamp.

State 1：Having Stop:

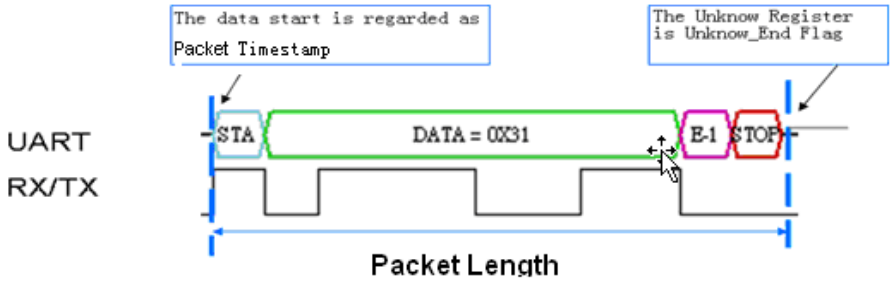


Fig4-83 - Packet Length

State 2: No Stop:

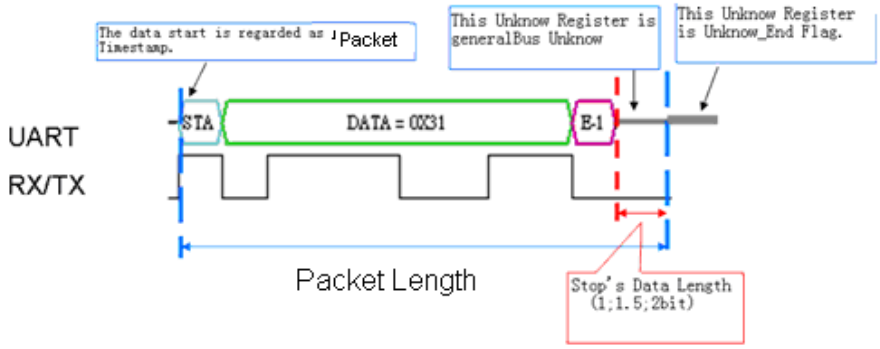


Fig4-84 - Packet Length

If the STOP falls short of condition, it isn't noted down in UART.

Packet Length: From START TimeStamp to Unknow_End Flag TimeStamp.

Packet Idling Length: From Unknow_End Flag TimeStamp to START TimeStamp.

4.5.4 SPI Analysis

SPI Introduction

SPI (Synchronous Peripheral Interface) is a parallel synchronous full duplex protocol with a Bus-like physical interface. This protocol was first developed by Motorola and was generally used for EEPROM, ADC, FRAM, and display device drivers which are equiped with low data transmission speed. The SPI data transmission is synchronous in both receiving and transmitting directions. Although Motorola initially did not define the clocking impulse, it is commonly seen that the clocking impulse is according to the master processor. In practice, there are two clocking impulses: CPOL (Clock Polarity) and CPHA (Clock Phase). The configuration of both CPOL and CPHA decides the sampling rate. When the SPI must transmit serial data, it initiates the highest bit.

Since SPI is a synchronous communication protocol and data transmission may not be in bytes, a complete SPI signal packet must consist of SCK, MOSI, MISO, and SS segments with CPHA and CPOL. They are as following.

SCK: Serial Clock Line (SCL).

MOSI: Master data output, Slave data input (MOSI stands for Master-Out-Slave-In).

MISO: Master data input, Slave data output (MISO stands for Master-In-Slave-Out).

SS: SS stands for Signal Selector of the master device which is to select signals for the Slave devices.

CPHA: The clock phase (CPHA) control bit selects one of the two fundamentally different transfer formats.

CPOL: The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock.

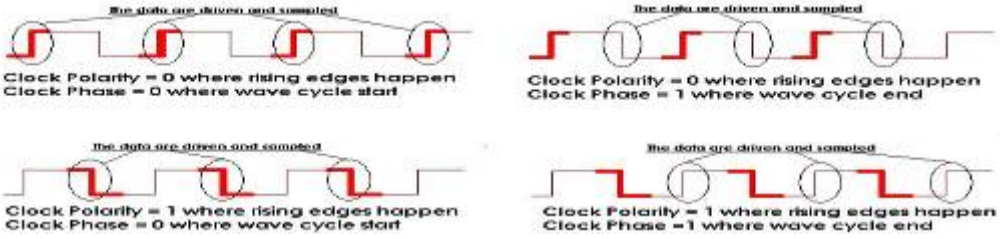


Fig 4-85 – Clock Polarity and Clock Phases

4.5.4.1 Software Basic Setup of Protocol Analyzer SPI

Step 1. Set up RAM Size, Frequency, Trigger Voltage and Trigger Position as described in Section 4.1.

Step 2. Set up the Falling Edge on the signal of SS which connected to the Signal Selector (SS) pin of the tested SPI board.

Step 3. Set up the Protocol Analyzer Dialog Box which is set as the steps of IIC.

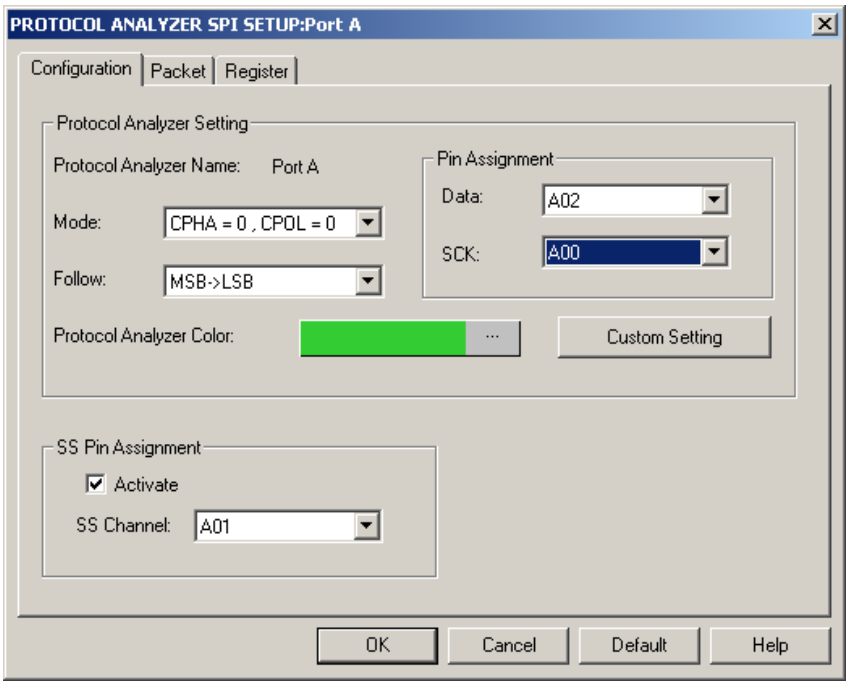


Fig 4-86 – SPI Setup

Step 4. SPI Setup

1. Protocol Analyzer Setting
   Select the Mode from the pull-down menu of "Port A".
   Then select MSB -> LSB or LSB -> MSB from the pull-down menu of the "Follow" to meet the specifications of the tested SPI circuit.
   Next click the to set the Protocol Analyzer Color.

Tip: Select MSB -> LSB to arrange data from left to right, eg. 0-0-0-1=0001; select LSB -> MSB to arrange data from right to left, eg. 1-0-0-0=0001.

2. Pin Assignment Setting
   Set the Data and SCK channels.
   Choose one channel from the pull-down menu of the Data to set the Data channel.
   Choose one channel from the pull-down menu of "SCK" to set the SCK channel.
3. SS Pin Assignment
   Click Activate on SS (Signal Selector).
   Then select the Signal which connects to the Signal Selector pin of the SPI DUT from the pull-down menu of "SS Channel".
4. Custom Setting
   A. SS Pin Assignment is activated.
      Click the Custom Setting, and the dialog box of the SPI Custom Setting will appear as shown in Fig 4-87.
   (1) Select "High" or "Low" to define the **SS enable level** of the tested SPI circuit..
   (2) Then type the number of the Data bit for the Bus signal.
   (3) Press **OK** to confirm the setup of SPI Custom Setting and return to the dialog box of the SPI Setting. (Tip: Press Default to give up the current Setup conditions)

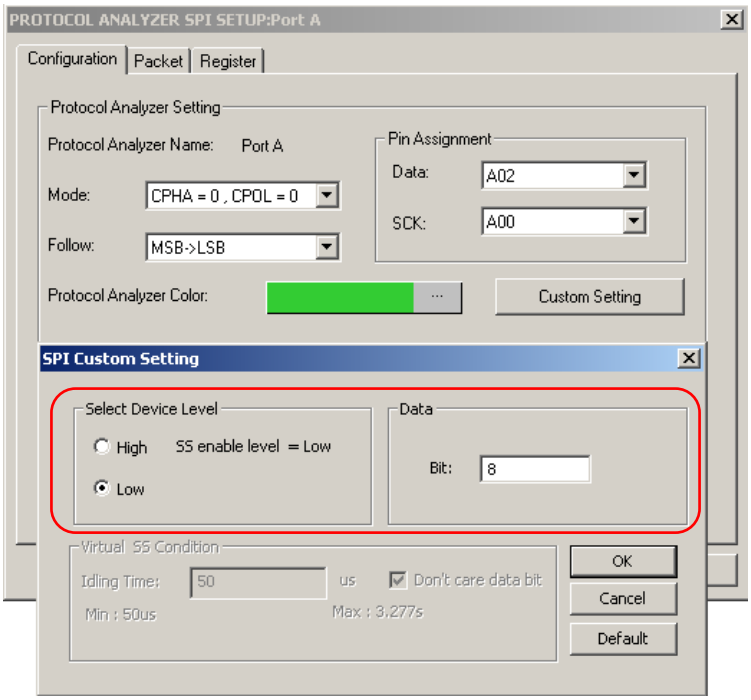


Fig 4-87 – SPI Custom Setting

B. SS Setting is not activated.
Click the Custom Setting, and the dialog box of the SPI Custom Setting will appear as shown in Fig 4-88.

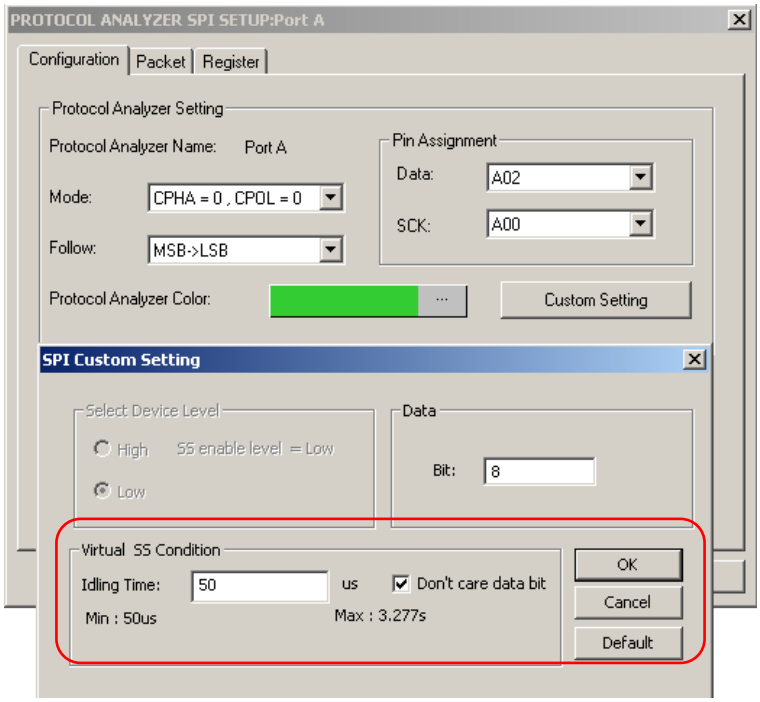


Fig 4-88 – Virtual SS Condition

(4) Type the Idling Time of the SCK signal on the tested SPI circuit. The Idling Time is defined as shown in Fig 4-89.

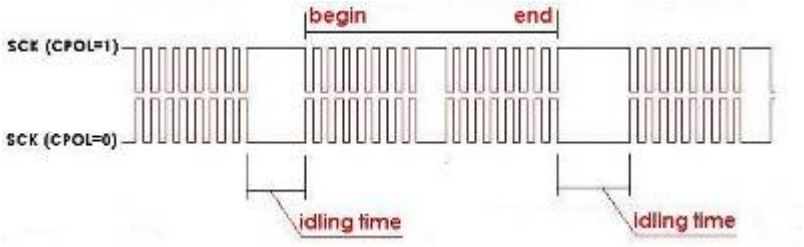


Fig 4-89 – Idling Time

(5) Click on the "Don't care data bits" function. The system will restart and count from the beginning of the data bits when the condition of the IdlingTtime set is qualified.

(6) Click off the "Don't care data bits" function. The system will decode the data stream until the bits of the data are received completely, when the condition of the Idling Time set is qualified.

(7) Press **OK** to confirm the setup of SPI Custom Setting and return to the dialog box of the SPI Setting. (**Tip:** Press **Default** to reset the current Setup conditions)

Step 5. Click **OK** to exit the dialog box of SPI setting.

Step 6. Click **Run** to acquire the SPI signal from the tested SPI circuit.

Tip: Click icon to view all the data, and then select the waveform analysis tools to analyze the waveforms.

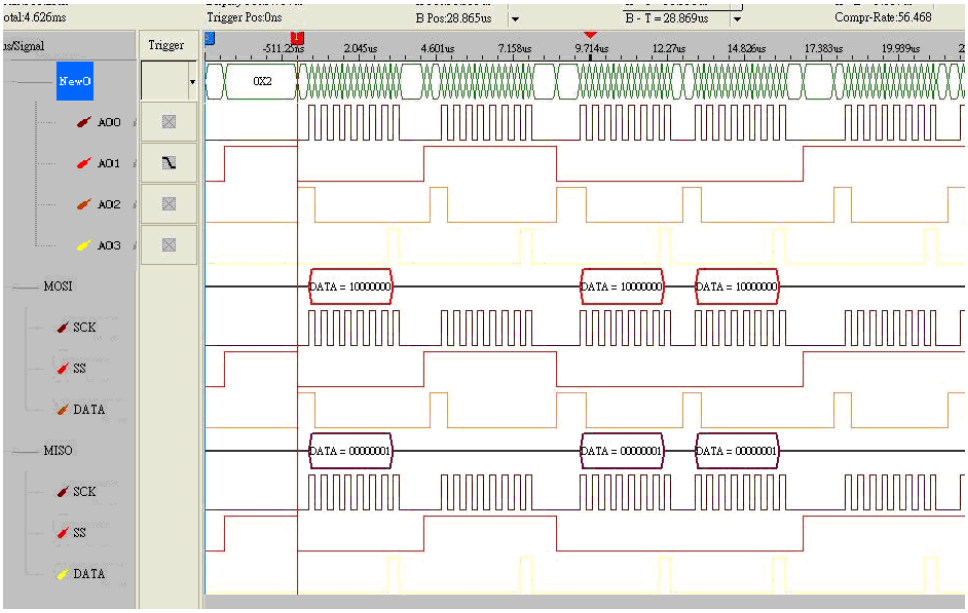


Fig 4-90 – SPI Waveform

4.5.4.2 Protocol Analyzer SPI Packet Analysis

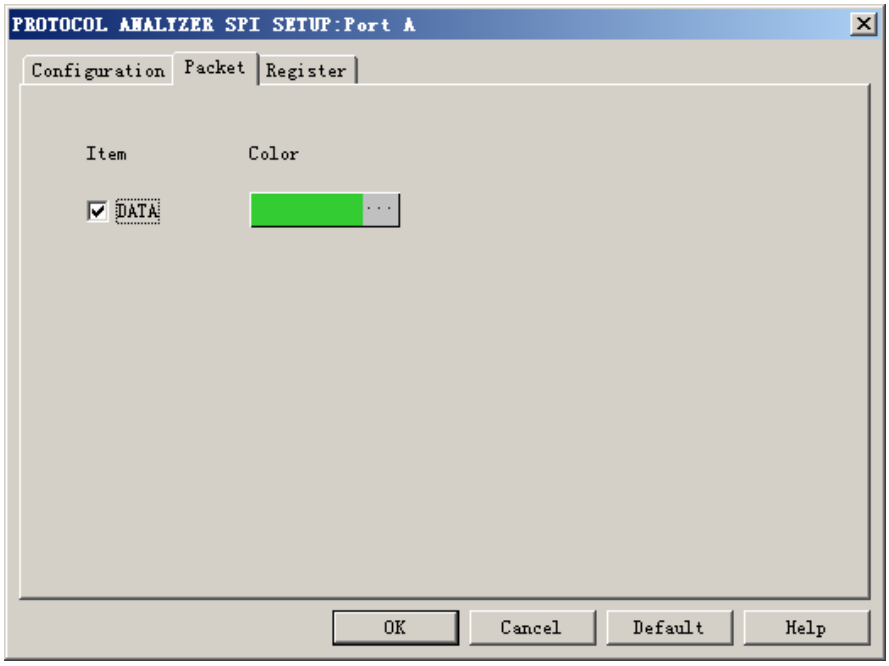


Fig4-91 - Protocol Analyzer SPI Packet

Data: List Data field captured by Bus in the packet display.

BUS Packet List View:

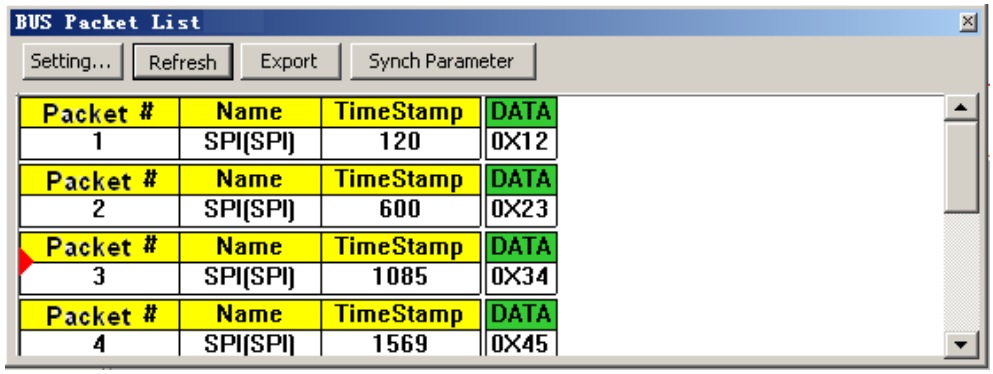


Fig4-92 - Protocol Analyzer SPI Packet List

Packet Length and Packet Idling Length

1. SS channel is activated.

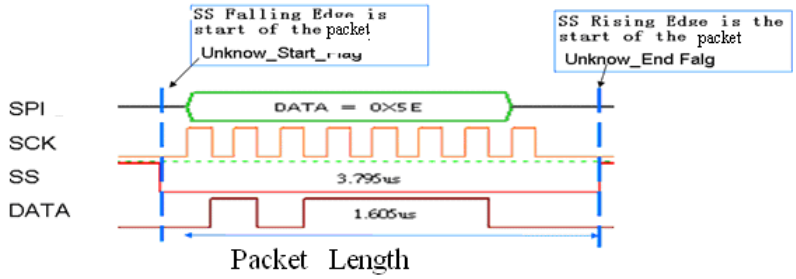


Fig4-93 - Packet Length

Packet Length: From Unknow_Start_Flag TimeStamp to Unknow_End Flag TimeStamp.

Packet Idling Length: From Unknow_End Flag TimeStamp to Unknow_Start_Flag TimeStamp.

2. SS channel is not activated.

Virtual SS is activated 1: Data is 8-bit; the Idling Time is set as 3us.

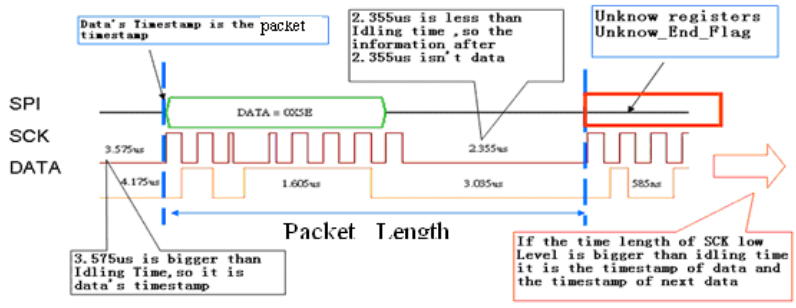


Fig4-94 - Packet Length

Packet Length: From Unknow_Start_Flag TimeStamp to Unknow_End Flag TimeStamp.

Packet Idling Length: From Unknow_End Flag TimeStamp to Unknow_Start_Flag TimeStamp.

Virtual SS is activated 2: Data is 8-bit; the Idling Time is set as 3us. **Don't care data bit** is not activated.

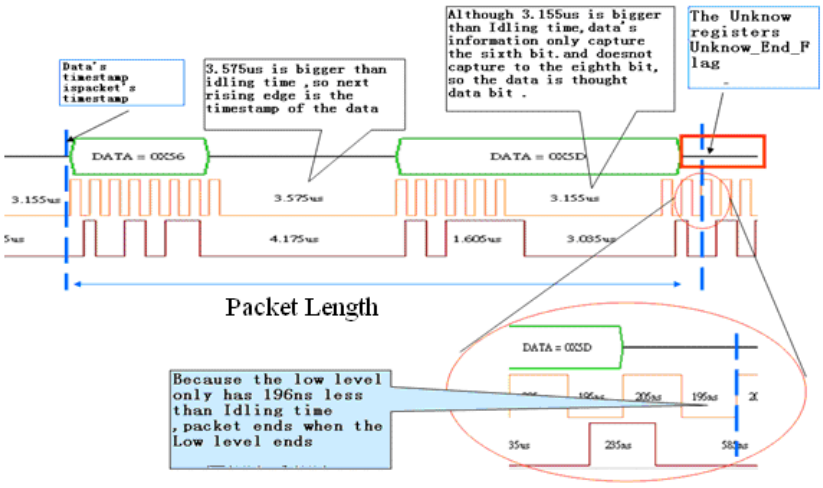


Fig4-95 - Packet Length

Packet Length: From Unknow_Start_Flag TimeStamp to Unknow_End Flag TimeStamp.

Packet Idling Length: From Unknow_End Flag TimeStamp to Unknow_Start_Flag TimeStamp.

Virtual SS is activated 3: Data is 8-bit; the Idling Time is set as 3us. **Don't care data bit** is activated.

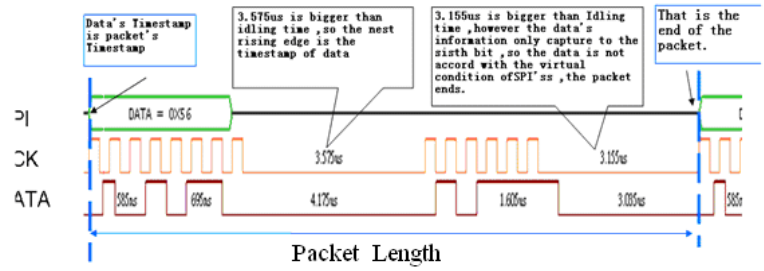


Fig4-96 - Packet Length

Packet Length: From Packet's TimeStamp Data to next Packet's TimeStamp Data.

Packet Idling Length: It is 0.

The End dot is Unknow.

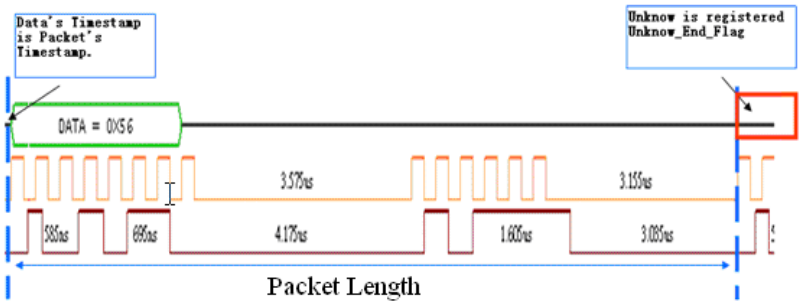


Fig4-97 - Packet Length

Packet Length: From Packet's TimeStamp Data to next Packet's TimeStamp Data.

Packet Idling Length: It is 0.

4.5.5 1-WIRE Analysis

Preface

To increase the Protocol Analyzer feature in order to analyze the Protocol Analyzer 1-WIRE transmission protocol data. Using LA analysis function, the required serial data can be converted and presented in the form of Bus. Therefore, the software needs to add a dialog box so as to set up a Protocol Analyzer 1-WIRE dialog box.

1-WIRE Introduction

1. Brief Introduction

Features

1-WIRE is a non-synchronic half-duplex serial transmission, which requires only one OWIO to transmit data. The typical 1-WIRE transmission structure is illustrated in Figure4-98. During the 1-WIRE transmission, the OWIO can be used to transmit data and supply power to all devices connected to the 1-WIRE . OWIO will link to a 4.7K Ohm Pull-High electric resistance which is linked to the power supply (3V-5.5V). The transmission speed for 1-WIRE can be divided into two types, Standard and High speed. Every 1-WIRE has a unique 64-bit code for the device to recognize. Therefore, the maximum number of link devices is 1.8; almost unlimited.

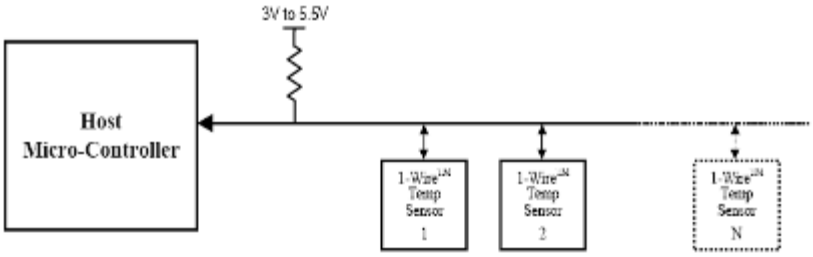


Fig4-98 - Applications

Applications

1-WIRE is commonly applied to the EEPROM and to certain sensor interfaces.

2. Protocol Analyzer Signal Specifications

Parameter	Value
Name of Protocol Analyzer	1-WIRE
Required No. of Channels	1
Signal Frequency	Not fixed, around 10K
Appropriate Sampling Rate	1MHz
Same Data Time Per Bit?	□Yes ■No
Name of Syn. Signals	OWIO
Data Verification Point	30 us after the falling edge signals

3. Protocol Analyzer IO Description

Name	Function
OWIO	The only I/O transmits Reset signals and data.

4. Protocol Analyzer Electrical Specifications

Parameter	Min	Typ	Max	Unit	Note
High-count Voltage	2.8		5.2	V	Every IC varies according to the Pull-High voltage.
Low-count Voltage		0		V	

Protocol Analyzer 1-WIRE Format Description

Two speed types of 1-WIRE: Standard: 1MHz (1us) High: 5MHz (0.2us)
Four types of 1-WIRE Signals:

1. Reset:
   Every communications period starts with Reset signal. Master will send a Reset Pulse so that all the Slave devices on the Protocol Analyzer 1-WIRE enter into recognition status. When one or many Slaves receive Reset Pulse, a Presence Pulse signal will be sent back from Slave, indicating receipt of the signal.
2. Write 0: Send a "0" bit to Slave (Write 1 time slot).
3. Write 1: Send a "1" bit to Slave (Write 1 time slot).
4. Read Data:
   "Read data sequences" resembles "Write time slot." However, when Master releases Protocol Analyzer and reads data from Slave devices, Master creates samples from Protocol Analyzer status. In this way, Master can read any 0 or 1 bit from Slave devices.

Four signal types are described respectively in the following:

1. **Reset**:

(1) When Master starts communicating with Slave, Master first sends a low-count Reset Pulse (TX) of t_{RSTL} (Standard speed: 480us; High Speed: 48us) for a period of time.

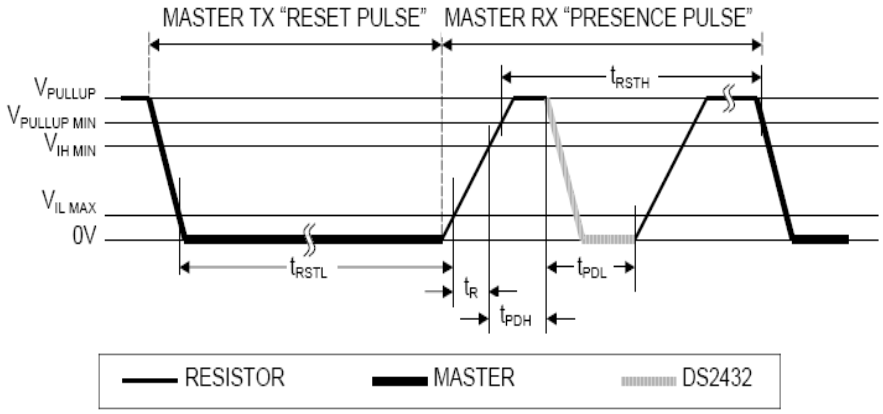


Fig4-99 - Master TX Reset Pulse and Master RX Presence Pulse

(2) Then, Master releases Protocol Analyzer and enters the RX mode. Through high- pull resistor, Protocol Analyzer 1-WIRE is pulled back to the high status.

(3) Then, Master detects a rising edge from the Data Line when every slave will wait for a period of time (t_{PDH}) (standard speed: 15-60us; high speed: 2-6us) and send back a Presence Pulse to Master (t_{PDL})(standard speed:60-240us; high speed: 8-24us).

(4) Finally, the Protocol Analyzer 1-WIRE will be pulled back to the high status through the resistor.

(5) Meanwhile, Master can detect any online Slave.

(6) From Fig4-100, the low count Reset Pulse and Presence Pulse signals can be clearly seen.

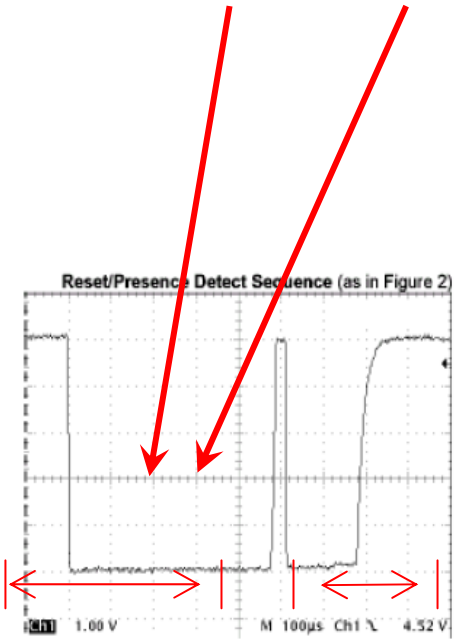


Figure 2a. You can clearly see the negative going reset and the presence pulse

Fig4-100 - Reset/Presence Detect Sequence

2. **Write Data**:

(1) To initialize Write Data, Master will convert the Data Line from the high logic to the low.

(2) There are two types of Write time slot: Write 1 Time Slot and Write 0 Time Slot.

(3) During a write cycle, all Write time slots must have duration of at least 60us and a recovery period of 1us.

When the I/O line goes down, Slave devices create samples from 15-60 us.

A. Write 0: If the sampling is low, 0 is generated as in fig4-101:

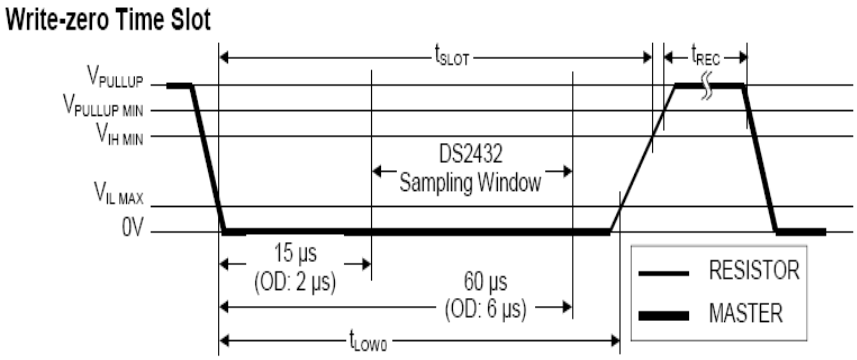


Fig4-101 - Write-zero Time Slot

B. Write 1: If the sampling is high, 1 is generated (note: Read 1 is of a similar wave form pattern) as in Fig4-102:

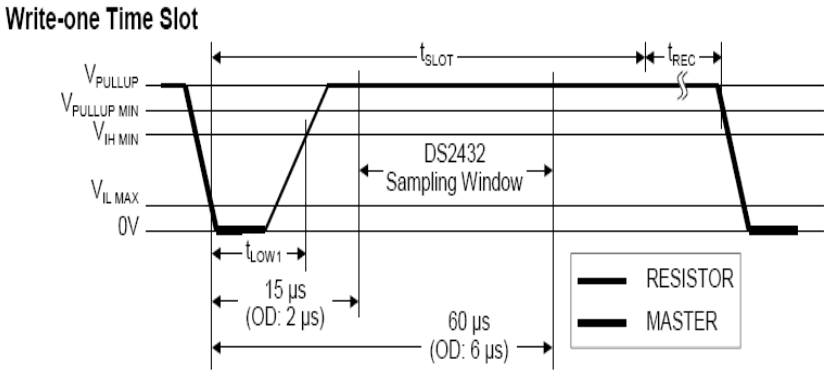


Fig4-102 - Write-one Time Slot

3. Read Data:

(1) When Slave reads data, Master will generate a Read time slot.

(2) To initialize Read Data, Master has to convert Data line from the high logic to the low.

(3) Data line must be kept as low as 1us.

(4) The Output Data of Slave must be 14us at most.

(5) To read from 15us where Read slot starts, Master must stop driving I/O.

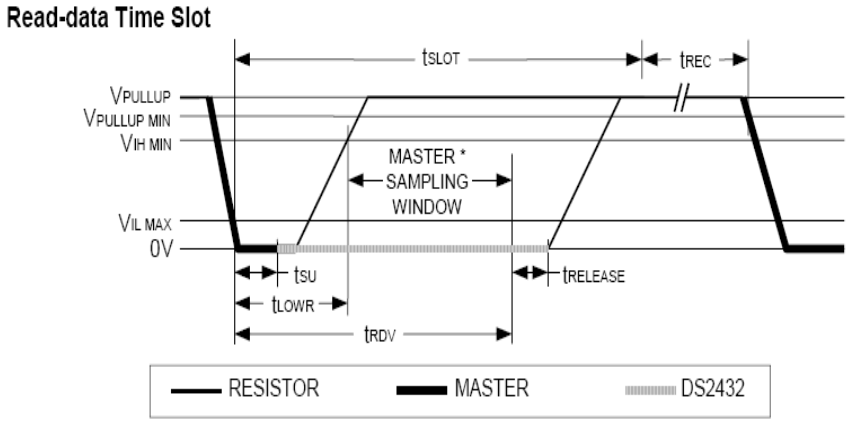


Fig4-103 - Read-data Time Slot

(6) When Read Time Slot ends, I/O Pin will be pulled back to the high count through the external resistor.

(7) During a write cycle, all Write time slots must have duration of at least 60us and a recovery period of 1us.

4. Typical 1-WIRE Conversation model can be summarized as below:

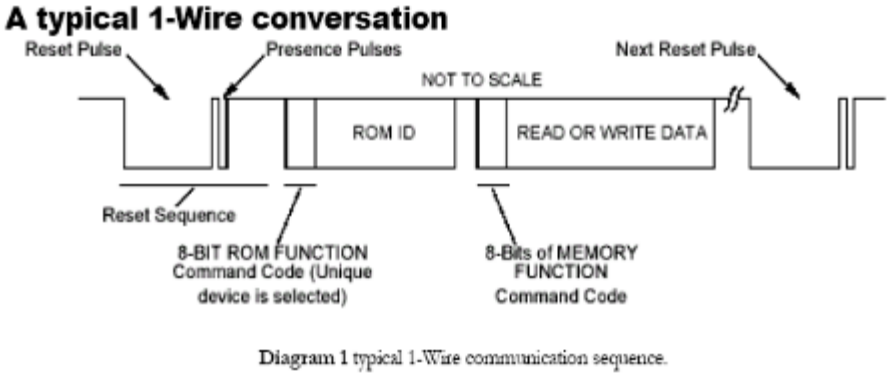


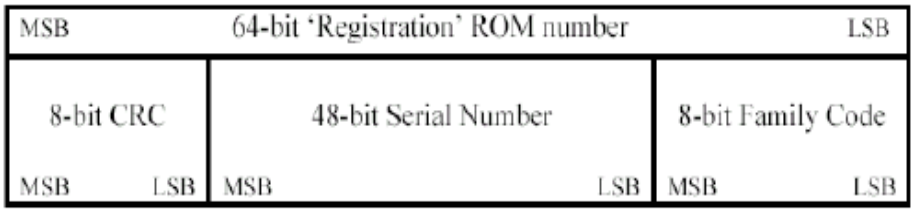
Diagram 1 typical 1-Wire communication sequence.

Fig4-104 - A typical 1-WIRE conversion

(1) Master keeps Protocol Analyzer at low signal (standard speed: 480us; high speed: 48us) as the Reset Pulse.
(2) Then, Master releases Protocol Analyzer and locates a Presence Pulse responded by any online Slave.
(3) The above two points are Reset Pulse and Presence Pulse, which can be put together as a Reset Sequence.
(4) If Presence Pulse is detected, the slave location will allow Master to access Slave using the Write 0 or Write 1 Sequence.

5. 1-WIRE Serial Number:

(1) Every 1-WIRE Slave has a unique laser memory.
(2) The serial number is 64bits.
(3) The serial numbers are 8bytes in total, located in three individual, which are illustrated as below:



(4) Starting from LSB, the first byte is for family code, which is used to identify product categories.
(5) Next, the 48bits is the only address for storage.
(6) The last byte, MSB is used to store CRC.

4.5.5.1 Software Basic Setup of Protocol Analyzer 1-WIRE

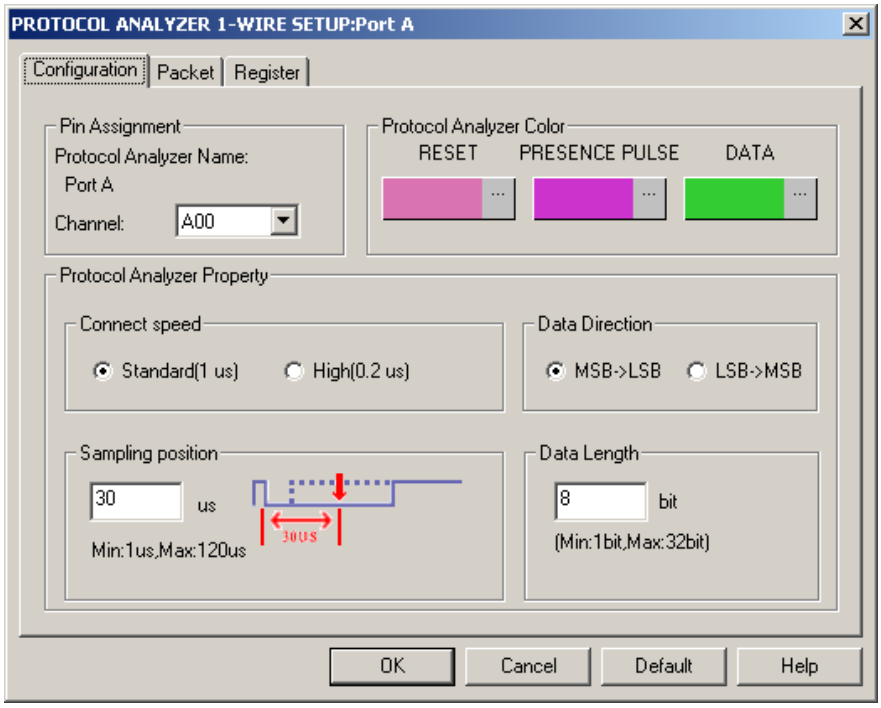


Fig4-105 - Protocol Analyzer 1-WIRE Setup

1. **Pin Assignment :**
   OWIO: Because there is only one channel for the signal, there are only two setup fields.
   Protocol Analyzer Name: Display the name of the selected Bus..
   Channel: The default is A00.
2. **Data Direction:**
   MSB->LSB: From high to low bits.
   LSB->MSB: From low to high bits.
3. **Connect Speed:**
   Standard: 1us.
   High: 0.2us.
4. **Protocol Analyzer Color:**
   RESET
   PRESENCE PULSE
   DATA

User Interface Instructions

Set up the Protocol Analyzer Dialog Box which is set as the steps of IIC.

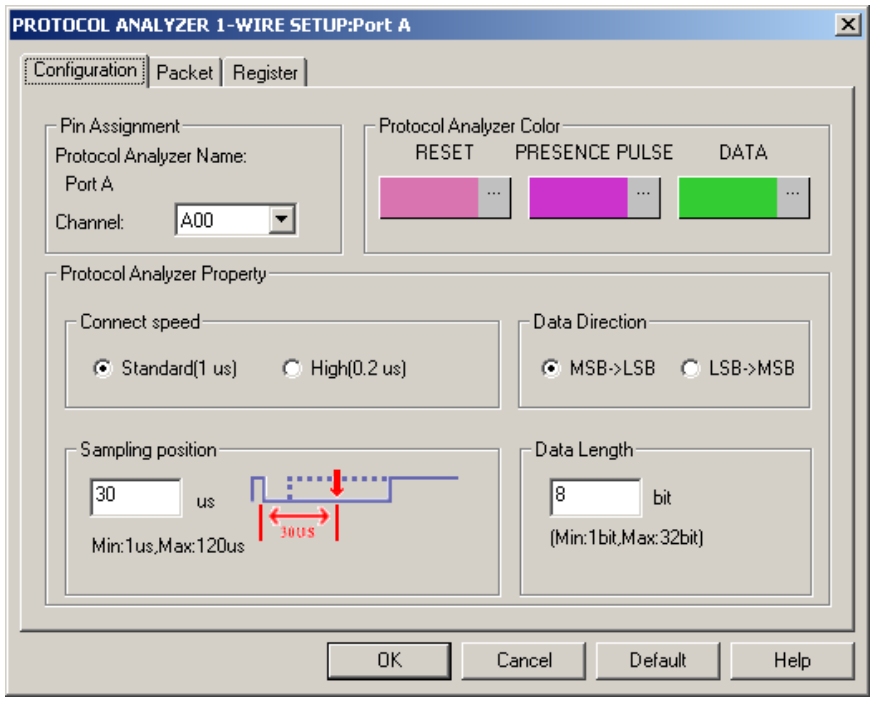


Fig4-106 - Protocol Analyzer 1-WIRE Setup

STEP 1. Select Channel

1-WIRE has only one IO. Select the channel that is to link to the IO.

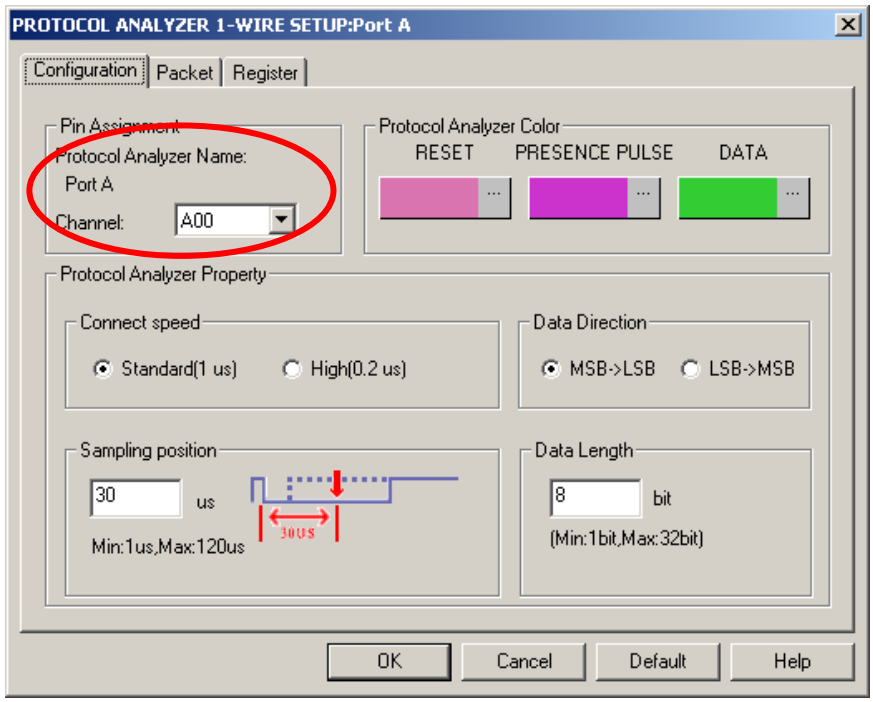


Fig4-107 - Protocol Analyzer 1-WIRE Channel Setup

STEP 2. Set Connect Speed

1-WIRE has two modes: Standard and High speed. The speed setup according to the specification of the object to be tested and the default mode is Standard.

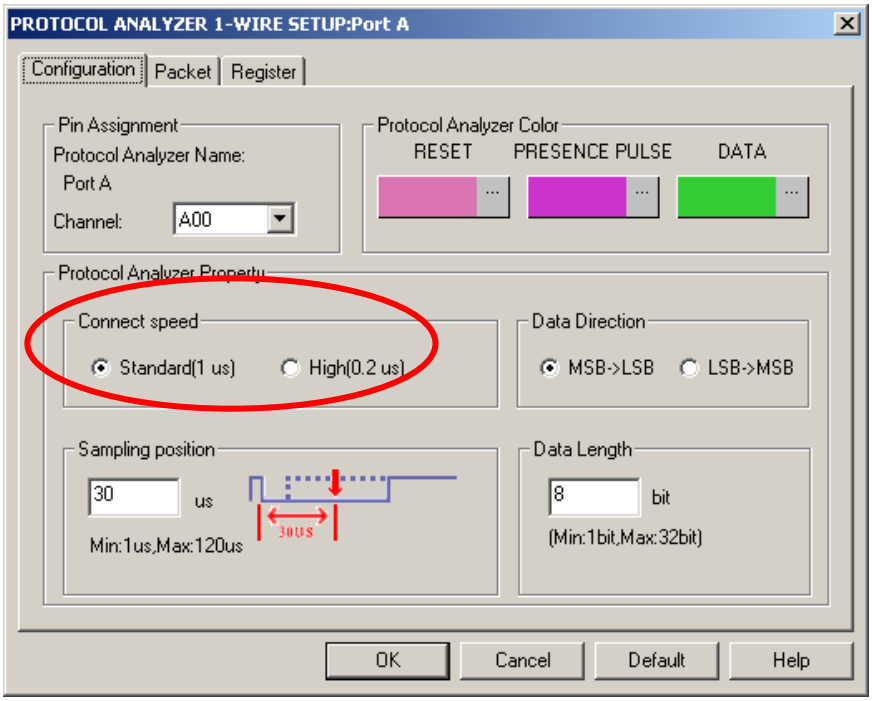


Fig4-108 - Protocol Analyzer 1-WIRE Connect Speed Setup

STEP 3. Set Data Direction

Set the Data Direction as either MSB -> LSB or LSB -> MSB.

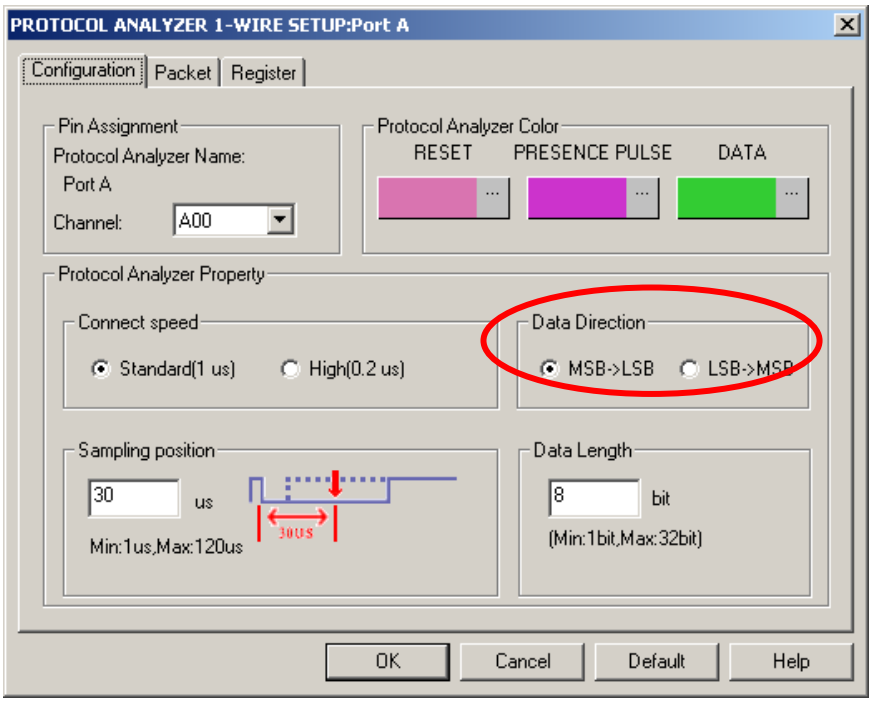


Fig4-109 - Protocol Analyzer1-WIRE Data Direction Setup

STEP 4. Set Sampling Position

Users can slightly adjust the sampling position of 1-WIRE. This feature is applicable when the signal cannot be decoded. The default value is 30us.

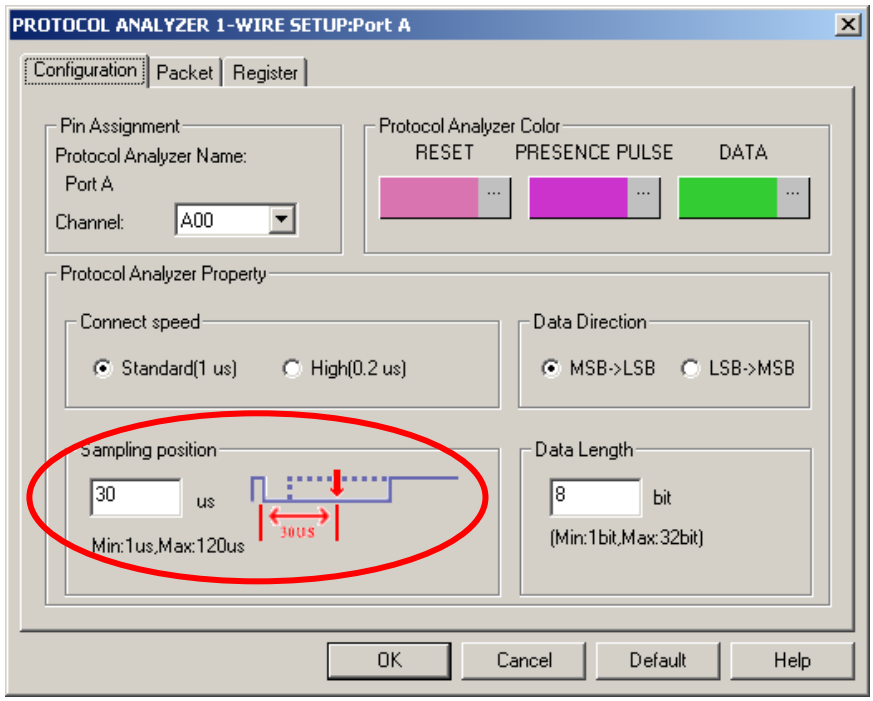


Fig4-110 - Protocol Analyzer 1-WIRE Sampling Position Setup

STEP 5. Set Data Length

This function decides how many bits of data can be combined as one set of figures. The default is 8 bits, and 32bits is the maximum.

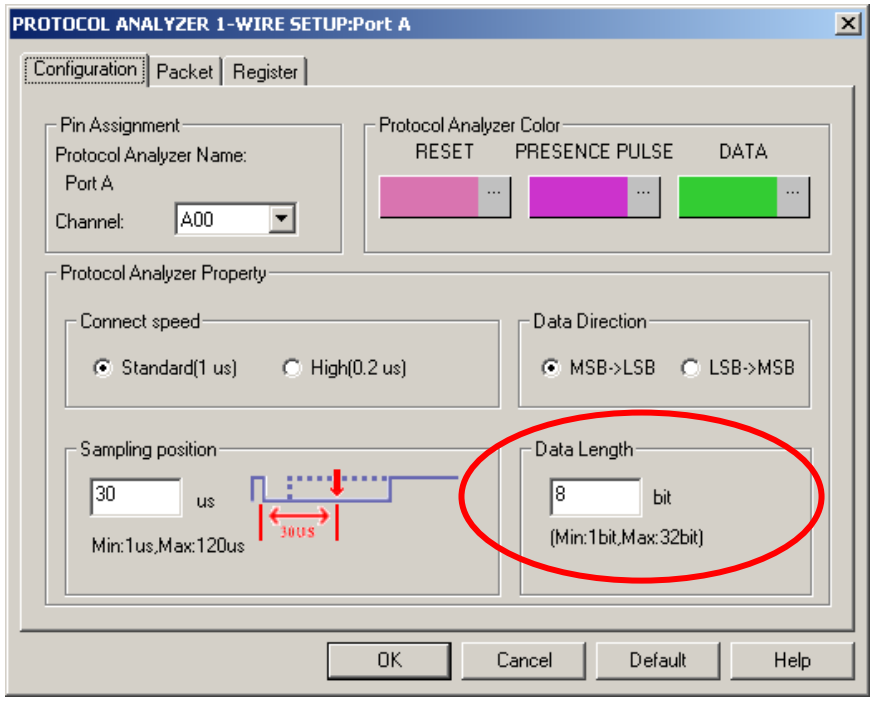


Fig4-111 - Protocol Analyzer 1-WIRE Data Length Setup

4.5.5.2 Protocol Analyzer 1-WIRE Packet Analysis

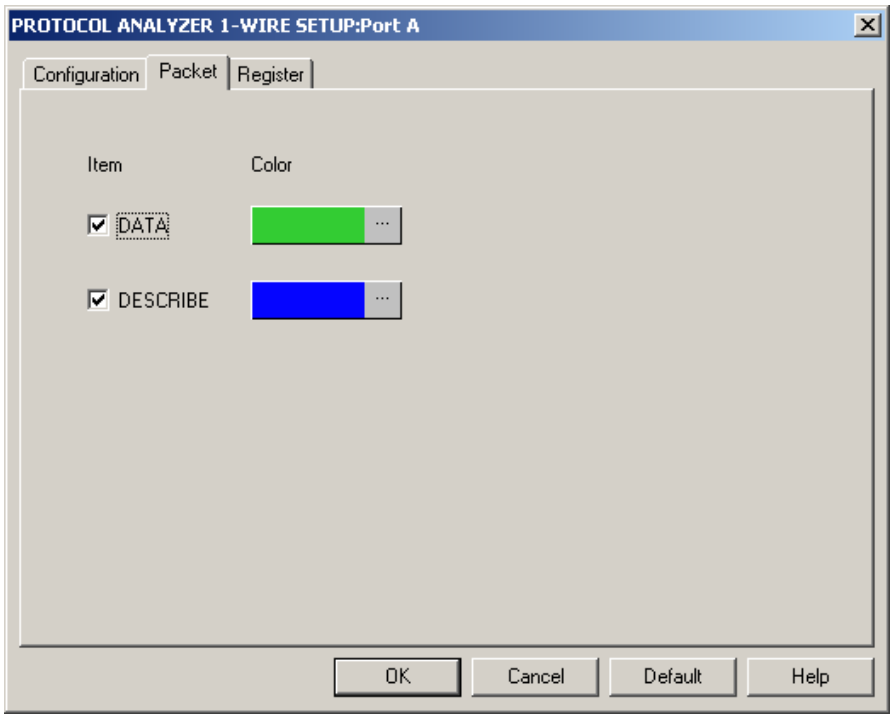


Fig4-112 - Protocol Analyzer 1-WIRE Packet

That is the new View; the below View includes several formats that 1-WIRE can happen; it describes Data number and Describe difference.

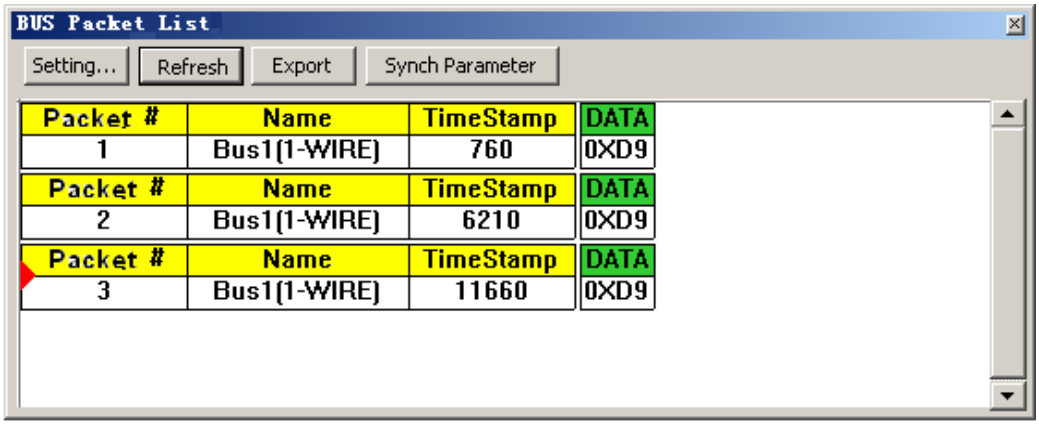


Fig4-113 - Protocol Analyzer 1-WIRE Packet List

Packet 1: It is commonly normal DATA which includes 1 DATA.

Packet 2: It is commonly normal DATA which includes 1 DATA.

Packet 3: It is commonly normal DATA which includes 1 DATA.

Packet and Idling Length: Packet's TimeStamp is reset.

4.5.6 HDQ Analysis

Preface

Increase the Protocol Analyzer feature to analyze the Protocol Analyzer HDQ transmission protocol data. Using LA analysis function, the required serial data can be converted and presented in the form of the Protocol Analyzer. Therefore, the software needs to add a dialog box so as to set up a Protocol Analyzer HDQ dialog box.

4.5.6.1 Software Basic Setup of Protocol Analyzer HDQ

HDQ Introduction

1. Brief Introduction

Features

Protocol Analyzer HDQ is a non-synchronic half-duplex serial transmission, which requires only one HDQ and uses a quasi-PWM (Pulse Width Modulation) to verify the serial data.

Applications

HDQ is commonly applied to the display interface for battery management.

2. Protocol Analyzer Signal Specifications

Parameter	Value
Name of Protocol Analyzer	HDQ
Required No. of Channels	1
Signal Frequency	Not fixed, around 12MHz, 13MHz and 19,2MHz
Appropriate Sampling Rate	100MHz
Same Data Time Per Bit?	□Yes ■No
Name of Syn. Signals	HDQ
Data Verification Point	Low signals＞190us converts to High signals＞40us

3. Protocol Analyzer IO Description

Name	Function
HDQ	The sole I/O transmits Host and BQ-HDQ status and data.

4. Protocol Analyzer Electrical Specifications

Parameter	Min	Type	Max	Unit	Note
Logic Input High	2.5			V	
Logic Input Low			0.5	V	

Protocol Analyzer HDQ Format Description

The format changes according to the pulse width, so the display must refer to the defined pulse width. Protocol Analyzer HDQ is made up of 16 bits signals. Firstly, after the period of status signals, a device will be installed for the 7 bits address through the Host so that 1-bit signals can be read or written. After a response time of high signals, the data will be exported in 8 bits format with the data and location content from LSB to MSB. The following is the Host to BQ-HDQ analysis.

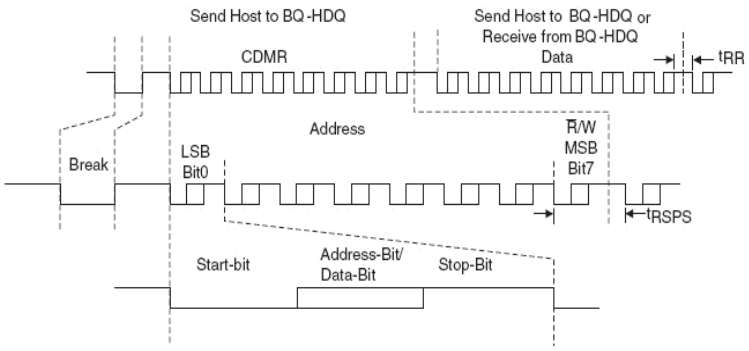


Fig4-114 - Host to BQ-HDQ Analysis

Protocol Analyzer Format

Break

This is the initial bit for the Protocol Analyzer HDQ: after Low signal lasting a period of t (B), it is then converted to a High signal lasting a period of t(BR). The length of Low signal is no less than 190us whereas the High signal is no less than 40us.

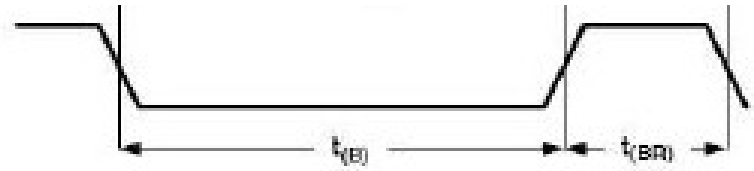


Fig4-115 - Pulse from Low to High

Address

The Address comprises 7 bits. The initial Low signal lasts a period of t(HW1) and if the write-0 status continues through the end of the t(HW0) period, the signal will convert to High and last throughout the period of t(CYCH), as shown by the dotted line in the following figure. Conversely, if it is the write-1 status, after t(HW1) period of time, the signal will convert to High and last throughout the period of t(CYCH), which is of 1 bit and no less than 190 us. The t(HW1) range is from 0.5us to 17us and no more than 50us. The t(HW0) range is from 86us to 100us and no more than 145us.

Read/Write

Read/Write is 1 bit. 0 and 1 are displayed in the same way as the above description.

T (RSPS)

The High signal lasts a period of 190us-320us. The following 8-bit data is from Send Host to BQ-HDQ or Receives from BQ-HDQ Data.

Data

Made up by 8 bits, it is from Send Host to BQ-HDQ or Receives from BQ-HDQ Data. It operates in the same way as in 2.2 and the data is from LSB to MSB.

BQ-HDQ To Host

If the data transmission is read by BQ-HDQ To Host, the initial Low signal lasts a period of t(DW1) and if the write-0 status continues through to the end of the t(DW1) period, the signal will convert to high and last throughout the period of t(CYCD), as shown by the dotted line in the following figure. Conversely, if it is the write-1 status, after t(DW1) period of time, the signal will rise and last throughout the period of t(CYCD), which is of 1 bit and ranges from 190us to 260us. The t(DW1) ranges from 32us to 50us and no more than 50us. The t(DW0) ranges from 80us to 145us.

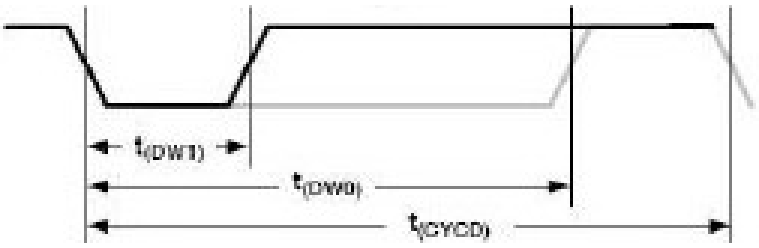


Fig4-116 - Signal from BQ-HDQ to Host

User Interface

Set up Dialog Box Description

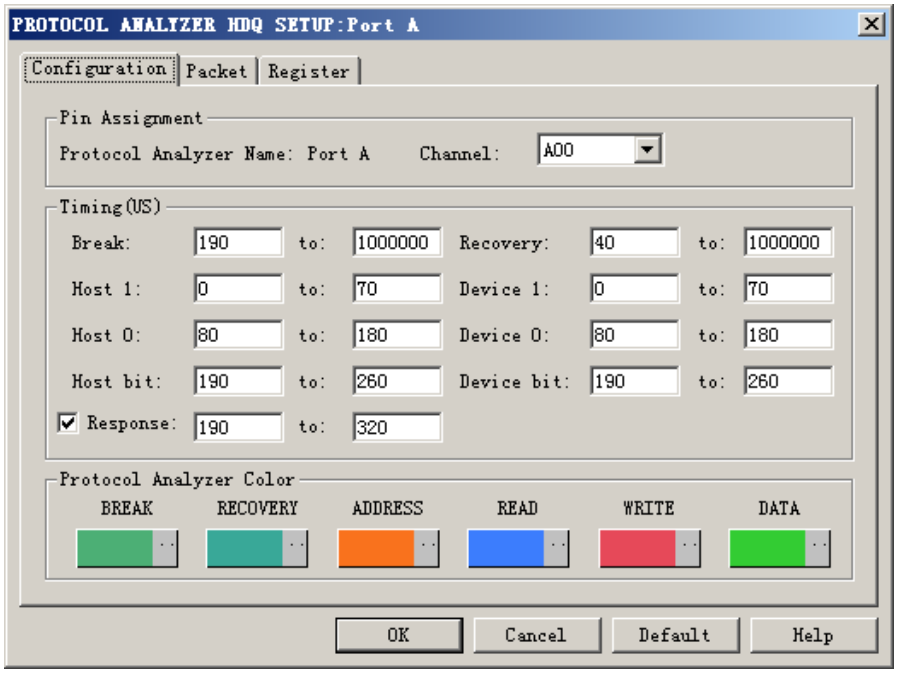


Fig4-117 - Protocol Analyzer HDQ Setup

1. **Pin Assignment:** HDQ has only one signal channel, therefore it only specifies the name of the channel and marks the selected channel.
   Protocol Analyzer Name: Display as HDQ.
   Channel: Preset as A00.
2. **Timing:**
   Set the time of BREAK, ADDRESS, READ, WRITE, DATA and RECOVERY.
3. **Protocol Analyzer Color:**
   BREAK
   RECOVERY
   ADDRESS
   READ
   WRITE
   DATA

Operating Instructions

Open the LAP operation interface.

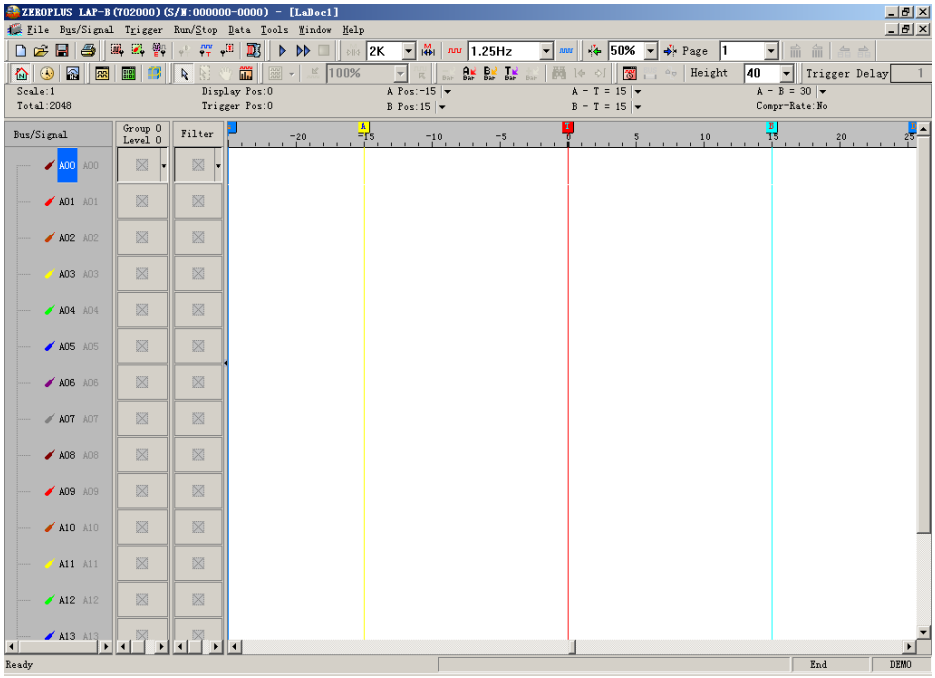


Fig4-118 - Operation Interface

Sample the HDQ waveform or open the sampled waveform.

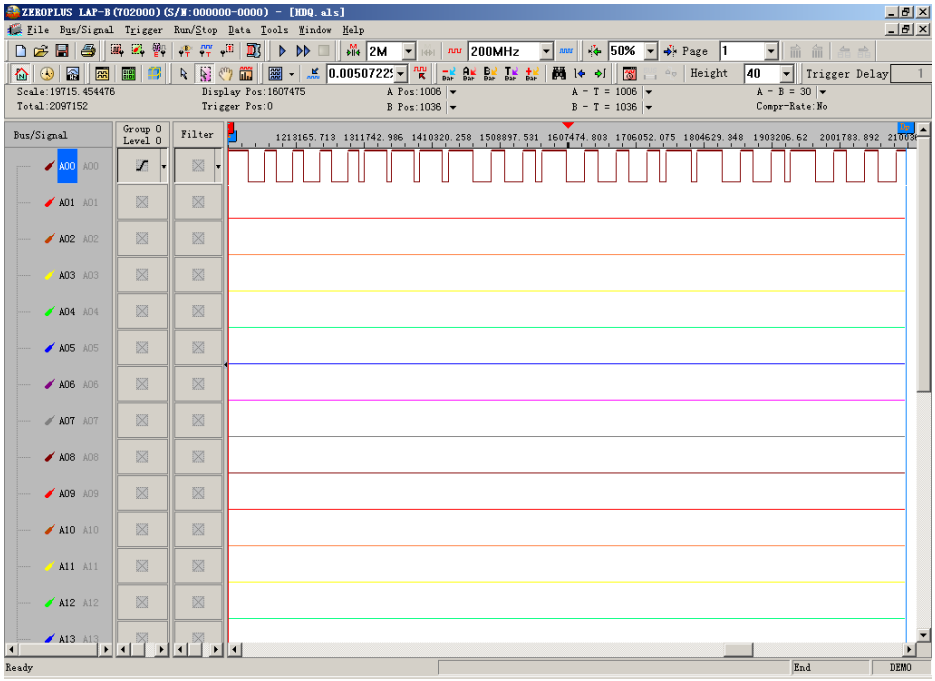


Fig4-119 - HDQ Waveform

Arrange the channels into Bus.

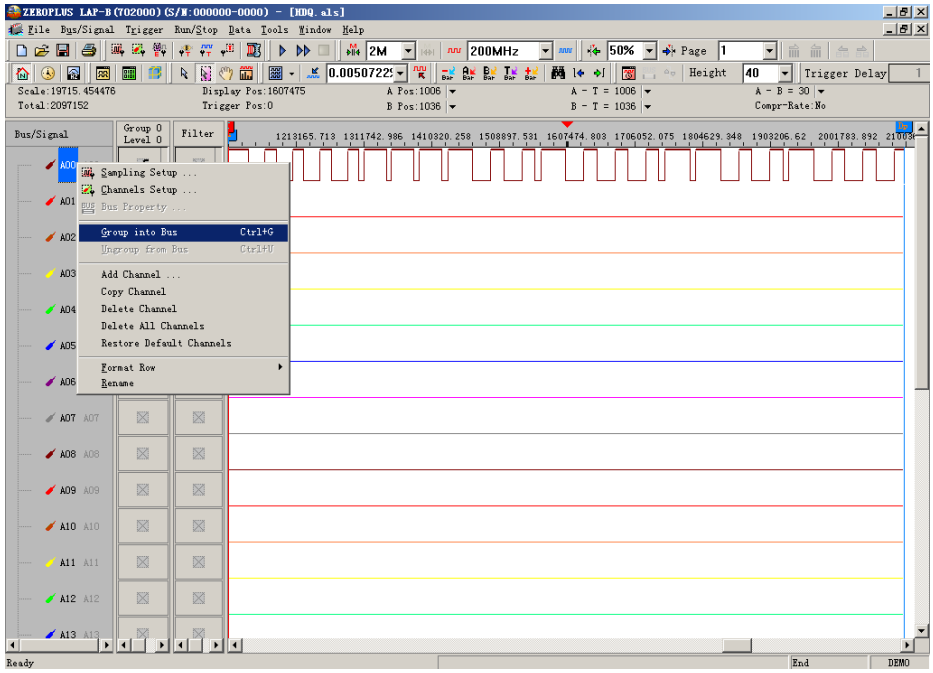


Fig4-120 - Group into Bus

Select Bus Property.

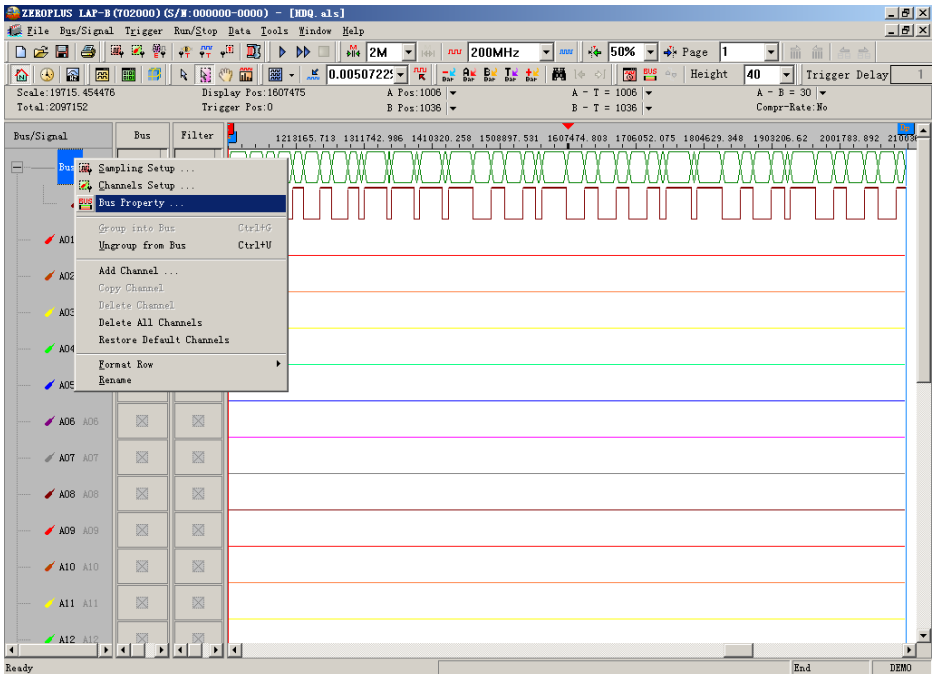


Fig4-121 - Bus Property

Select the decoding function of the Protocol Analyzer HDQ.

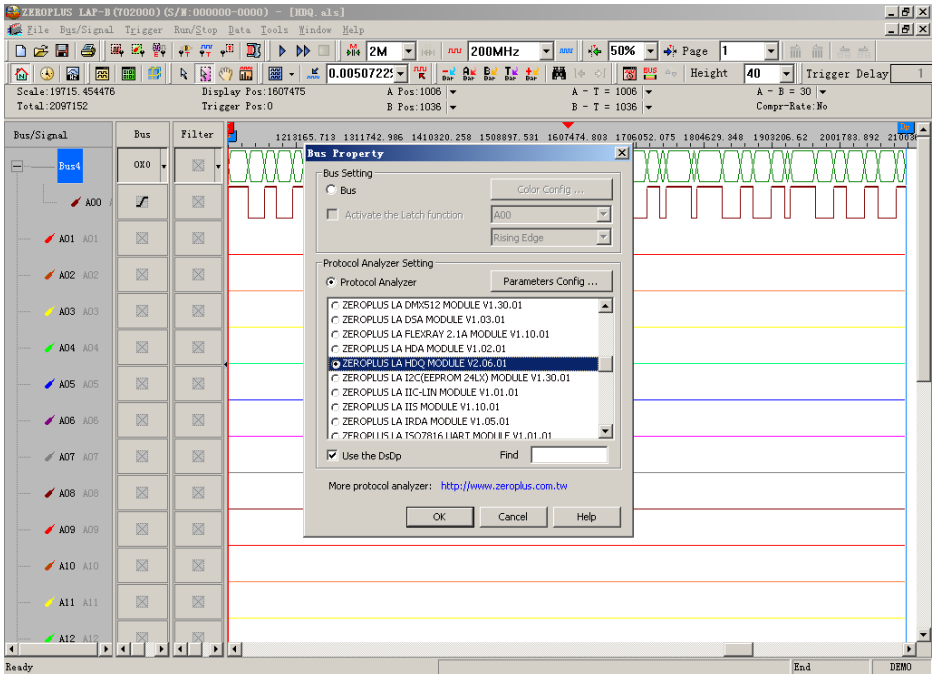


Fig4-122 - Protocol Analyzer HDQ Setup

Complete the Protocol Analyzer HDQ decoding.

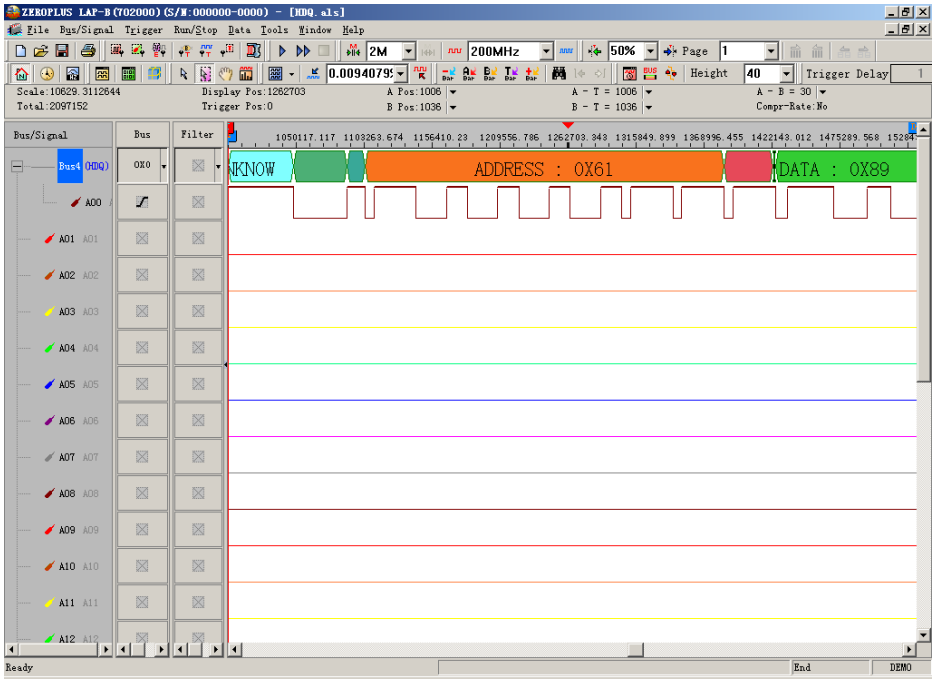


Fig4-123 - Protocol Analyzer HDQ Decoding

4.5.6.2 Protocol Analyzer HDQ Packet Analysis

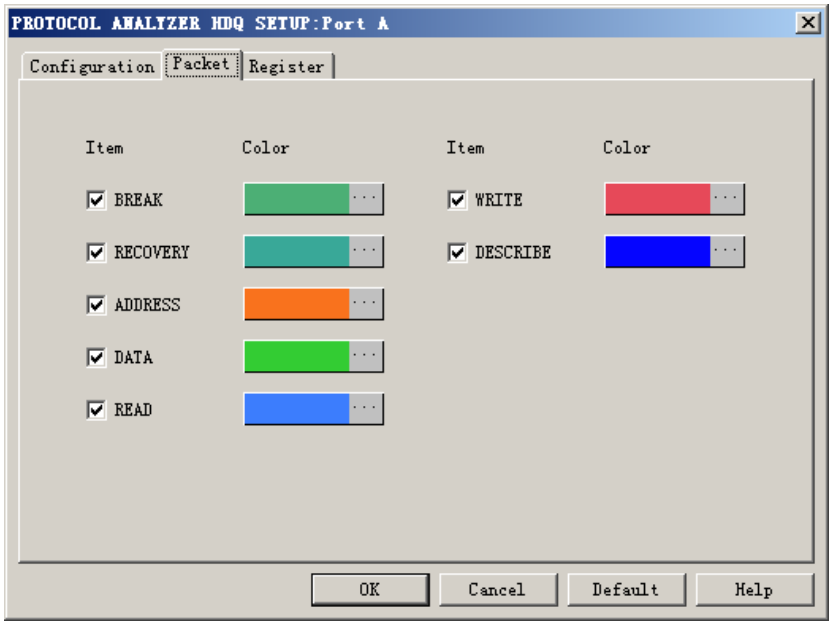


Fig4-124 - Protocol Analyzer HDQ Packet

Item: Select the content which needs to be displayed in the packet list, which includes BREAK, RECOVERY, ADDRESS, DATA, READ, WRITE and DESCRIBE.

Color: Set color for items which needs to be displayed in the packet list.

4.5.7 CAN2.0B Analysis

Preface

Add Protocol Analyzer function to analyze CAN 2.0B transport protocols data. CAN 2.0B serial transmission, there are two signal lines, CANH and CANL, which match with baud ratio judge serial data. If you want to change serial data into the Protocol Analyzer format, you need to analyze this function with LA. A dialog box needs to be added; you should set up a Protocol Analyzer CAN 2.0B dialog box.

4.5.7.1 Software Basic Setup of Protocol Analyzer CAN2.0B

CAN2.0B Introduction

1. Brief Introduction

Features

CAN2.0B(Controller Area Network) is an Asynchronous Transmission protocol. It costs low, sky-high use rate, far data transmission distance (10KM), very high data transmission bit(1M bit/s), sending information without appointed devices according to message frame, dependable error disposal and detection error rule, message automatism renewal after damage, and node can exit Bus function on the serious error .

Application

CAN2.0B is used for automotive electronics correlation systems connection.

2. Protocol Analyzer Signal Specifications

Parameter	Value
Name of Protocol Analyzer	CAN2.0B
Required No. of Channels	1
Signal Frequency	Not fixed, around 12MHz, 13MHz and 19,2MHz
Appropriate Sampling Rate	100MHz
Same Data Time Per Bit?	□Yes ■No
Name of Syn. Signals	CAN2.0B
Data Verification Point	Low signals＞190us convert to High signals＞40us

3. Protocol Analyzer IO Description

Name	Function
CANL	The main signal source of transmission data
CANH	Signal is opposite to the signal source of transmission data

4. Protocol Analyzer Electrical Specifications

Parameter	Min	Type	Max	Unit	Note
Logic Input High	2.5			V	
Logic Input Low			0.5	V	

CAN2.0B Frame Specification

CAN2.0B can separate frames as follows: Data Frame, Remote Transmit Request Frame, Error Frame, Overload Frame. Because CAN2.0B is transmitted by the format of difference signals, the signal can separate into CANL and CANH, and the signal direction of CANH is opposite to that of CANL, next we analyze CAN2.0B signal with the standard of CANL.

Basic Data Frame

Data frame can be divided into Basic CAN and Peli CAN, Data Frame of Basic CAN transmission. As follows, message data can be separated into Start of Frame(SOB), Arbitration Field, Control Field, Data Field, CRC Field, Ack Field, End of Frame.

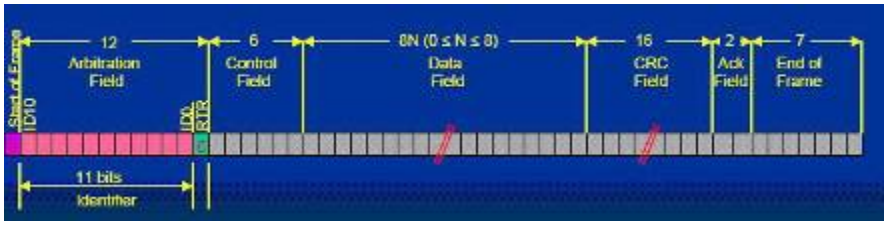


Fig4-125 - Basic Data Frame

Start of Frame

Every Start of Frame must be 0, which means asking far data to come back.

Arbitration Field

Identifier is 11bits; its function is the sequence when transmitting signal, numerical value is less, the priority is higher, and the array is from ID-10 to ID-0, and the numerical value is not all from ID-10 to ID-4, finally RTR(Remote Transmit Request) is the judgment bit of transmission or Remote Transmit Request. When RTR=0, it denotes that the data goes out; when RTR=1, it means asking far data to come back.

Control Field

Control Field consists of 6 bytes, including Data Length Code and two Reserved Bits as Peli frame for future expansion. The transmission reserved bit must be 0. Receiver receives all bits combining 1 with 0. As the below figure, IDE and RB0 of Control Field are reserved bits which must be 0 and the latter 4bits are only 0-8 which denotes the data behind will transmit several bytes data.

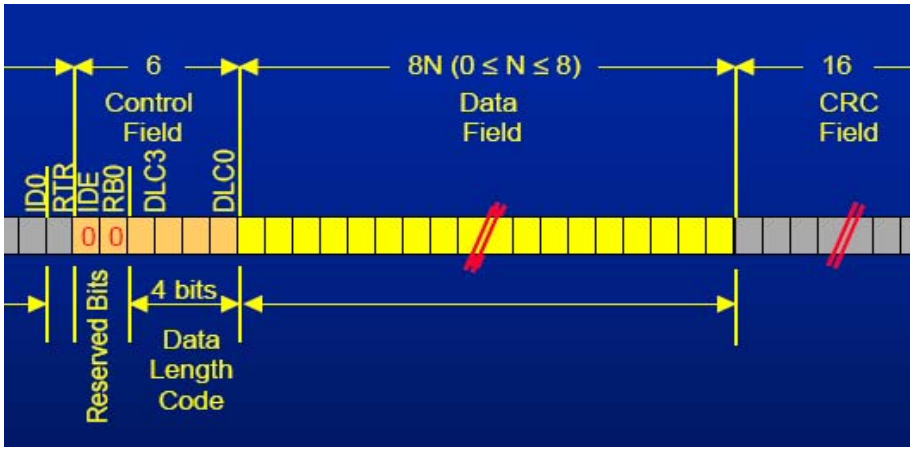


Fig4-126 - Control Field

Data Field

The Data Field consists of the data to be transferred within a Data Frame. It can contain from 0 to 8 bytes, and each contains 8 bits which are transferred MSB first.

CRC Field

16bits CRC, the last is a delimiter, and the default is 1.

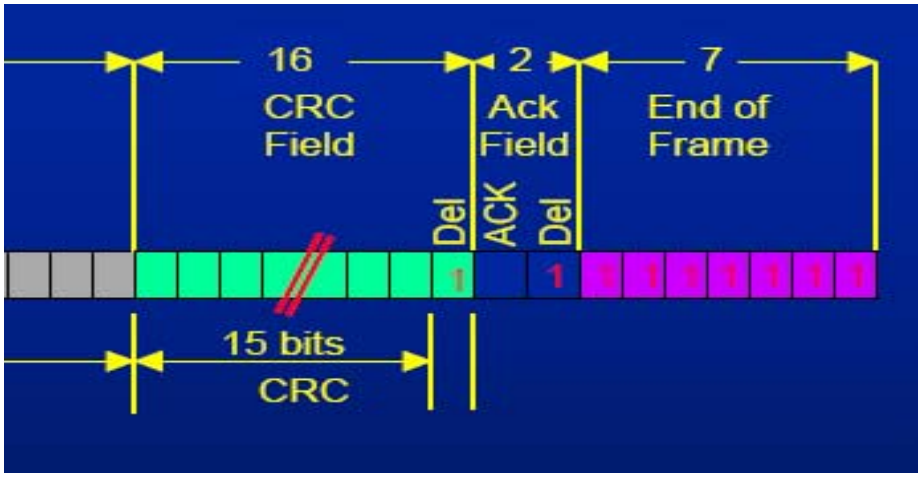


Fig4-127 - CRC Field

Ack Field

That is the return signal of Receiver, which has two bits, and the final is a delimiter whose default is 1. If receiving success, Ack will send back 0, then the transmitter knows the Receiver has received the data.

End of Frame

1111111 denotes End.

Peli Data Frame

In the Peli Data Frame , Data Frame as follows, the frame of message is separated into Start of Frame(SOB), Arbitration Field, Control Field, Data Field, CRC Field, Ack Field, End of Frame. However, the parts of Arbitration Field have much more than 18bits and the SRR and IDE is 1.

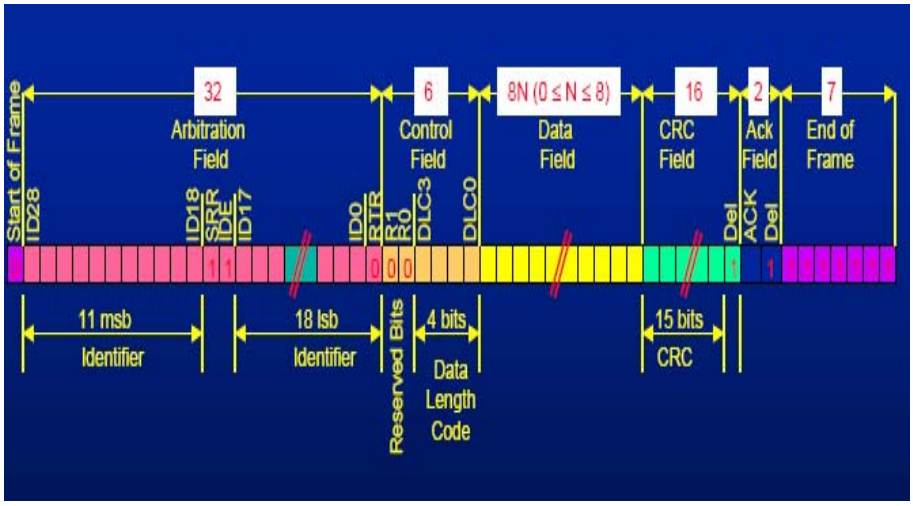


Fig4-128 - Peli Data Frame

Remote Transmit Request Frame

When RTR=1, it denotes Remote Transmit Request Frame, at this time, DLC3...DLC0 are the data bytes of return data. And the frame doesn't have Data Field.

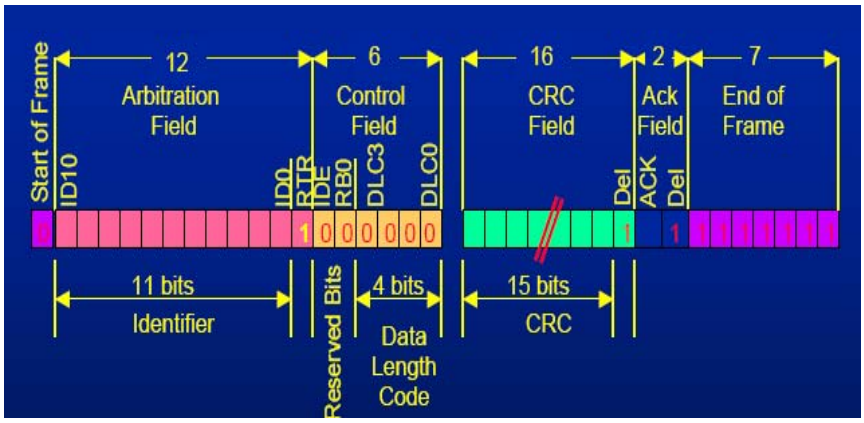


Fig4-129 - Remote Transmit Request Frame

Error Frame

The active Error Flag consists of six consecutive Data Field 'dominant'bits. Dominant bits violate the law of bit stuffing. All bits can produce Error Frame after recognizing bit stuffing wrong, which the Error Frame called Error. Corresponding Error flag field includes sequence bits from 6 to 12 (which produces by 1 or more nodes). Error Frame ends in Error Delimiter field. After Error Flag sends out Bus actively to get the right state, and the interrupted node tries its best to send abeyant message Error Delimiter: Error Delimiter consists of eight 'recessive' bits and allows Bus node to restart Bus transmission after Error happens.

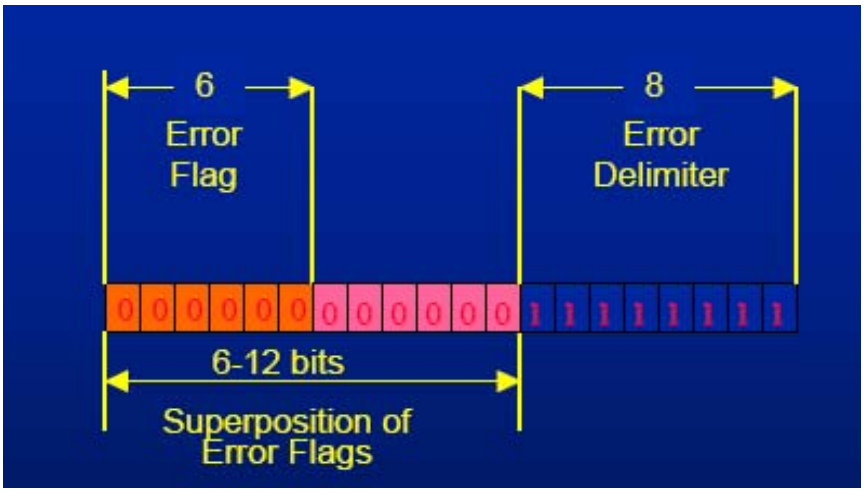


Fig4-130 - Error Frame

Overload Frame

There are two kinds of Overload conditions, which both lead to the transmission of an Overload Flag. The internal conditions of a node which requires a delay of the next Data Frame start during the first bit of Intermission. Overload Flag can send six '0', which may damage Intermission format so that it makes the other nodes know node sending Overload Flag at this time. When Overload Flag is sent out, Over Delimiter can send eight '1', others send seven '1' after finishing either.

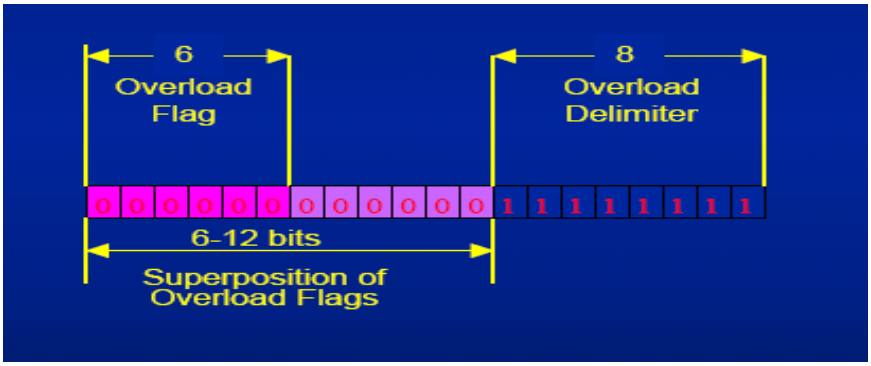


Fig4-131 - Overload Frame

Interframe Space

Interframe Space is divided into Intermission and Protocol Analyzer Idle. Intermission is three '1'. It is impossible to send any message during this time, excepting Overload Frame**.** The Protocol Analyzer is recognized to be free; the period of Protocol Analyzer Idle may be of arbitrary length. And any station having something to transmit can access the Protocol Analyzer. When a node is at the state of 'error passive', the node will send eight '0' after Intermission and other nodes have the chance to retransmit themselves information.

User Interface

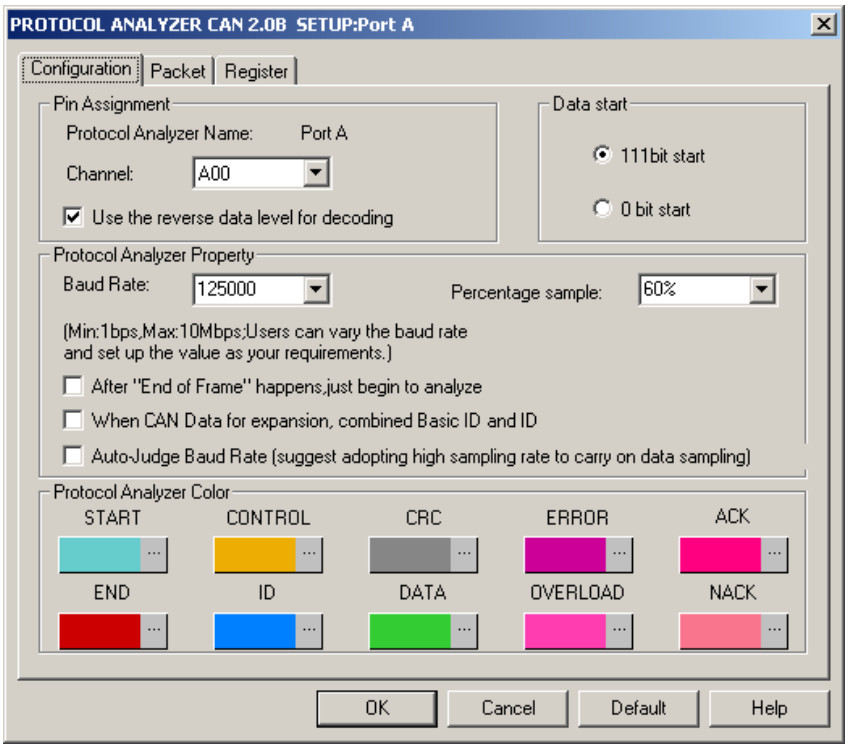


Fig4-132 - Protocol Analyzer CAN2.0B Setup

Pin Assignment: CAN 2.0B signal can be divided into CANL and CANH, and the default is CANL.
Use the reverse data level for decoding: Reverse the data.
Data Start: It can be divided into two forms, 111 bit start and 0 bit start.
Protocol Analyzer Property:
Baud Rate: Input baud rate by hand directly, and the baud rate is an integer. The default is 125000; the list includes 5, 10, 20, 40, 50, 80, 100, 125, 200, 250, 400, 500, 666, 800, 1000, 2000, 125000, etc. And the biggest one is 10M. Users can vary the baud rate and set the value as their requirements.
Percentage sample: This way needs to input position of sampling in baud rate; the default is 60%; the range is

25%~75%. And the default can be adjusted by 1%. The list is one option of interval 5%. If the below is selected, the decoding function can work after the end of the frame. Combination extends format: Progress Basic ID and ID.
Protocol Analyzer Color: START, CONTROL, CRC, ERROR, END, ID, DATA , OVERLOAD.

Operating Instructions

Turn on the user interface of Logic Analyzer.

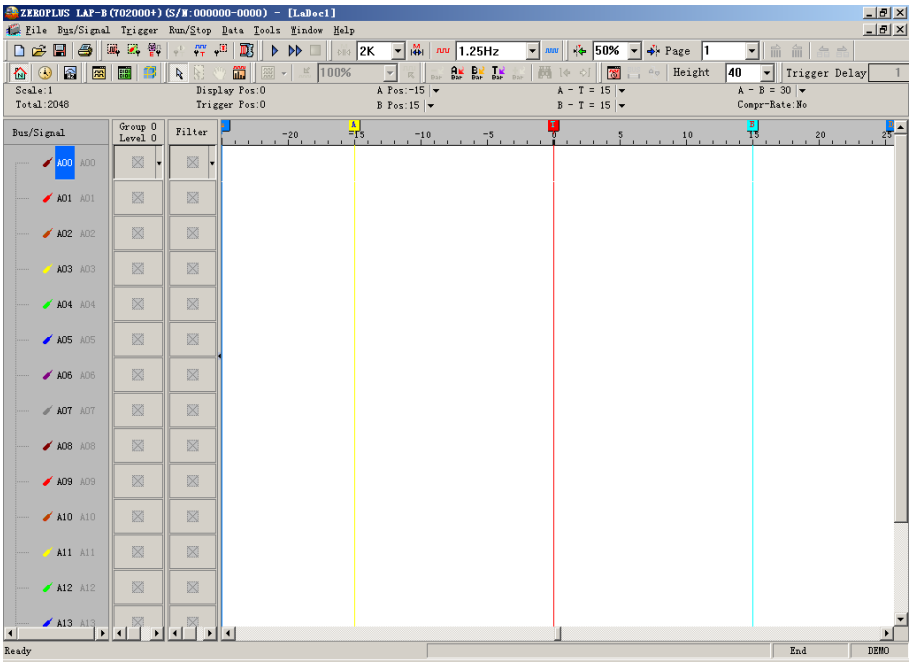


Fig4-133 - User Interface

Sample the CAN2.0B waveform or open the sampled waveform.

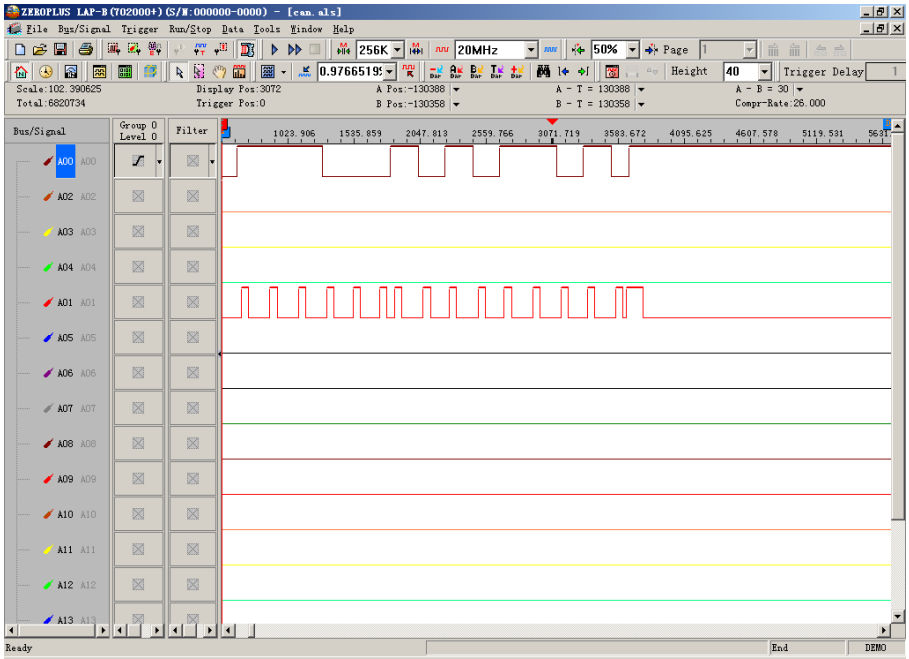


Fig4-134 - CAN2.0B Waveform

Group the channels into Bus.

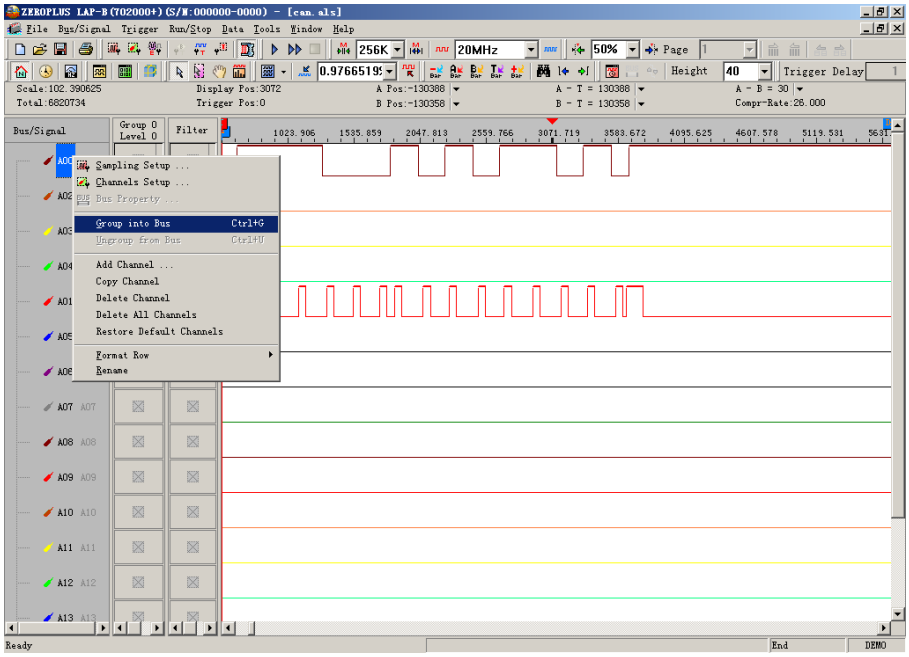


Fig4-135 - Group into Bus

Select the Bus Property to set up the Bus Property dialog box

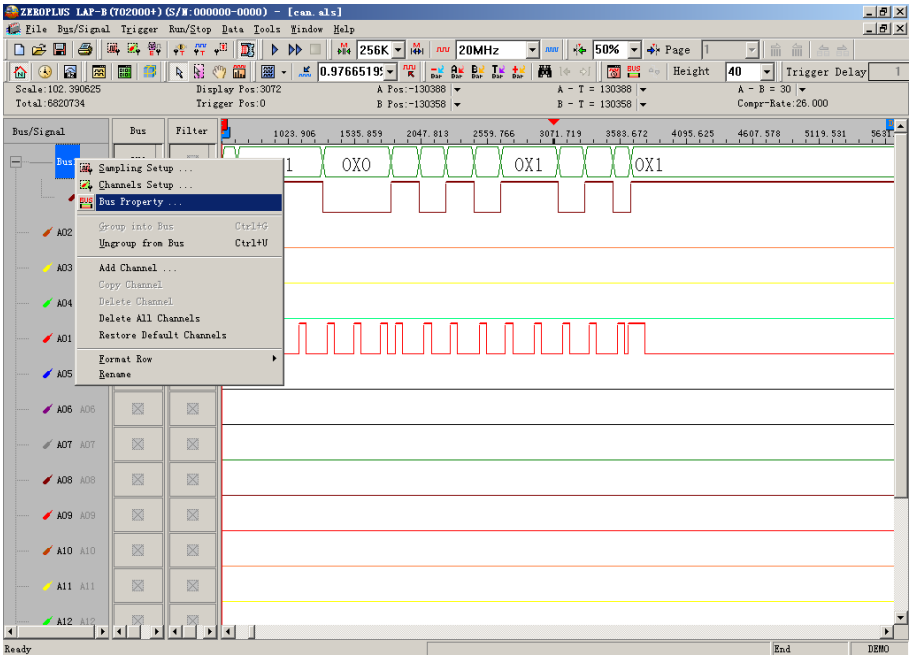


Fig4-136 - Bus Property

Select the decoding function of the CAN2.0B

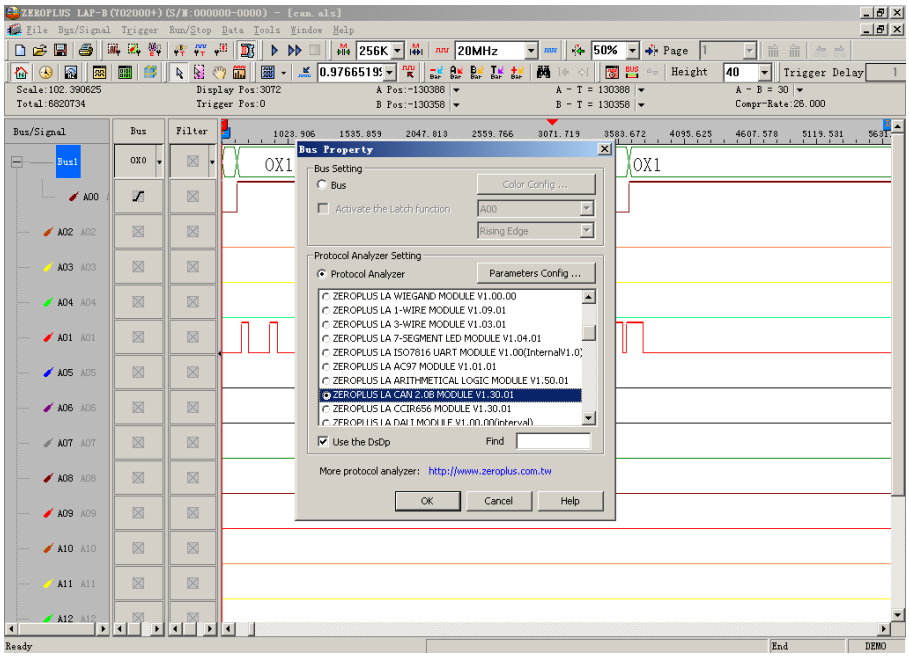


Fig4-137 - CAN2.0B Property Setup

Double click the ZEROPLUS LA CAN2.0B Module V1.30.01 to set up the Protocol Analyzer CAN2.0B.

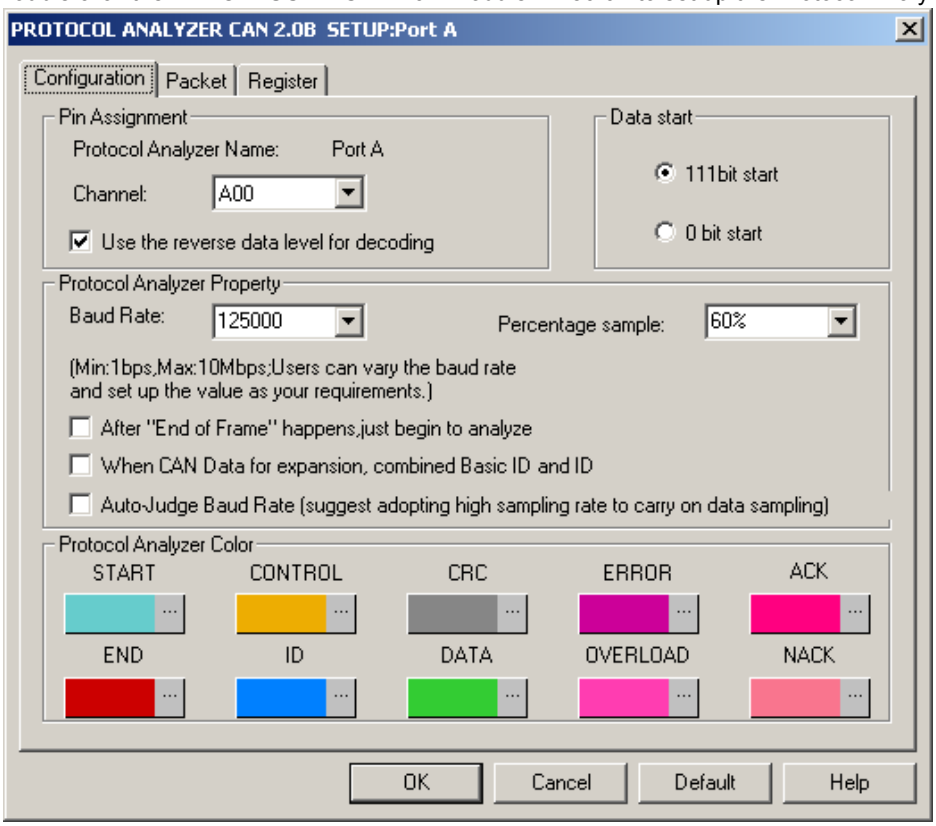


Fig4-138 - Protocol Analyzer CAN2.0B Setup

Click **OK** on the Protocol Analyzer CAN2.0B dialog box to complete the CAN2.0B Bus decoding.

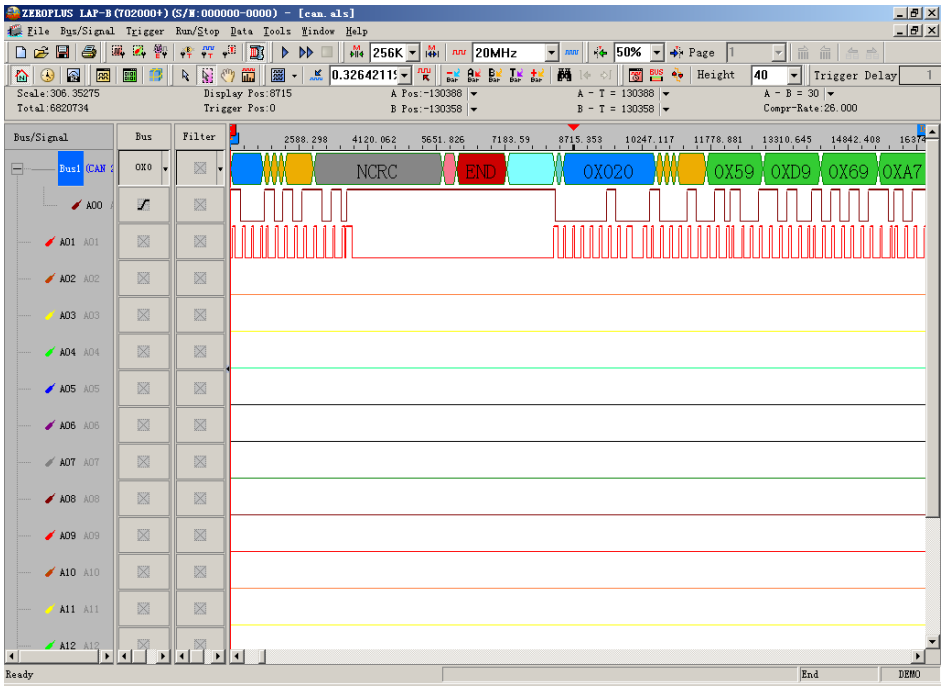


Fig4-139 - Protocol Analyzer CAN2.0B Decoding

4.5.7.2 Protocol Analyzer CAN2.0B Packet Analysis

Select Packet Item in the Protocol Analyzer CAN2.0B dialog box to set the packet.

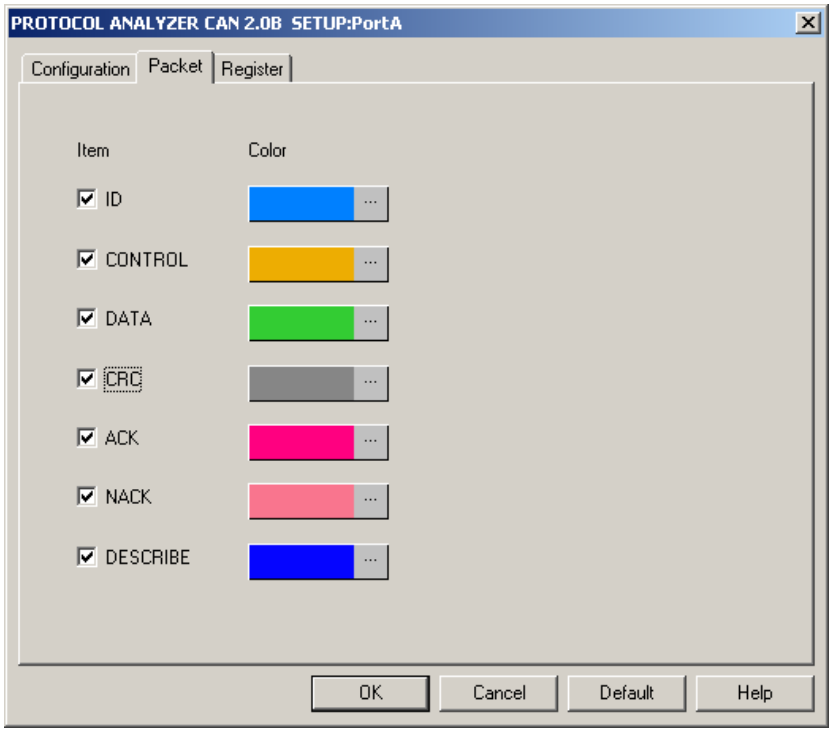


Fig4-140 - Protocol Analyzer CAN2.0B Packet

The packet color can be varied by users.

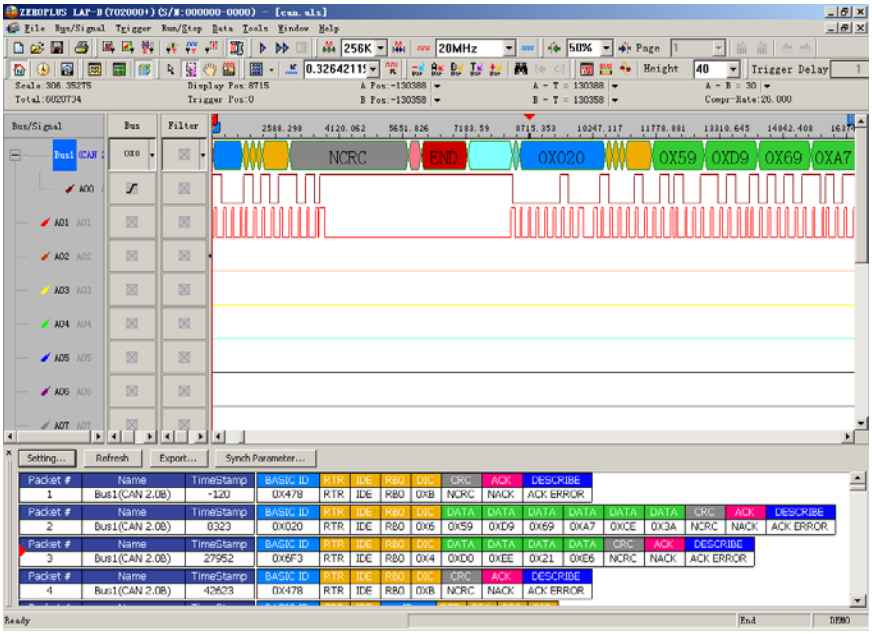


Fig4-141 - CAN2.0B Packet List Displayed under the Waveform

4.6 Compression

The compression function can make the system to compress the received signal and has more data stored in each memory channel.

4.6.1 Software Basic Setup of Compression

Step 1. Set up RAM Size, Frequency, Trigger Voltage and Trigger Position as described in Section 4.1.

Step 2. Set up the trigger edge on the signal or the bus to be triggered.

Step 3. Click icon, or click the compression function from the sampling setup dialog box then click **Apply** or **OK** to run.

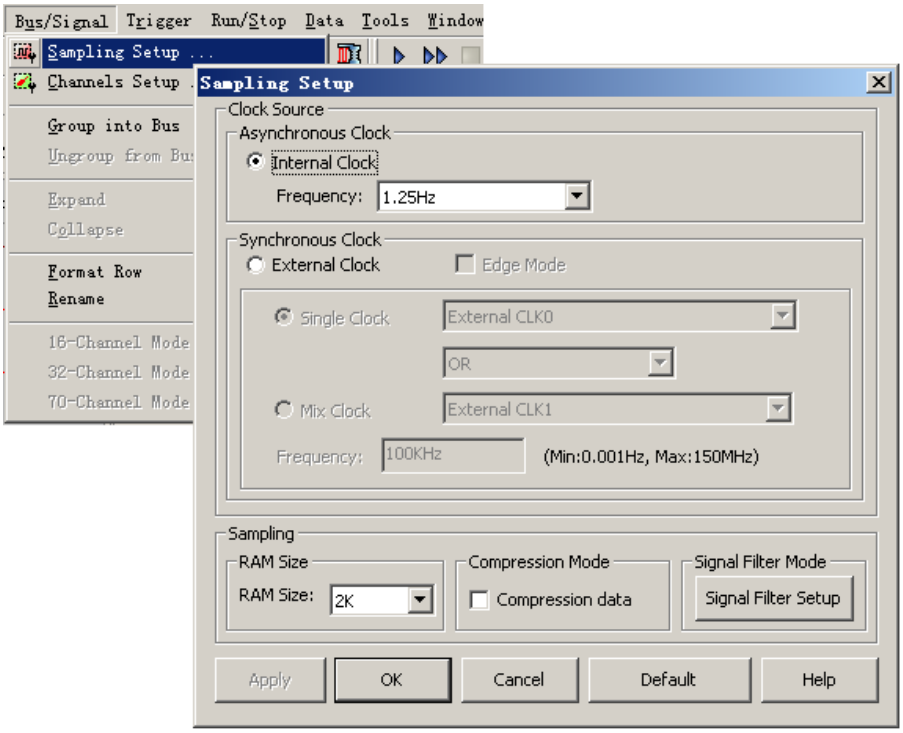


Fig 4-142 – Compression Mode

Step 4. Click **Run**, and then activate the signal from the tested circuit to acquire the result on the waveform display area. Fig 4-143 shows the result before and after compression has been applied.

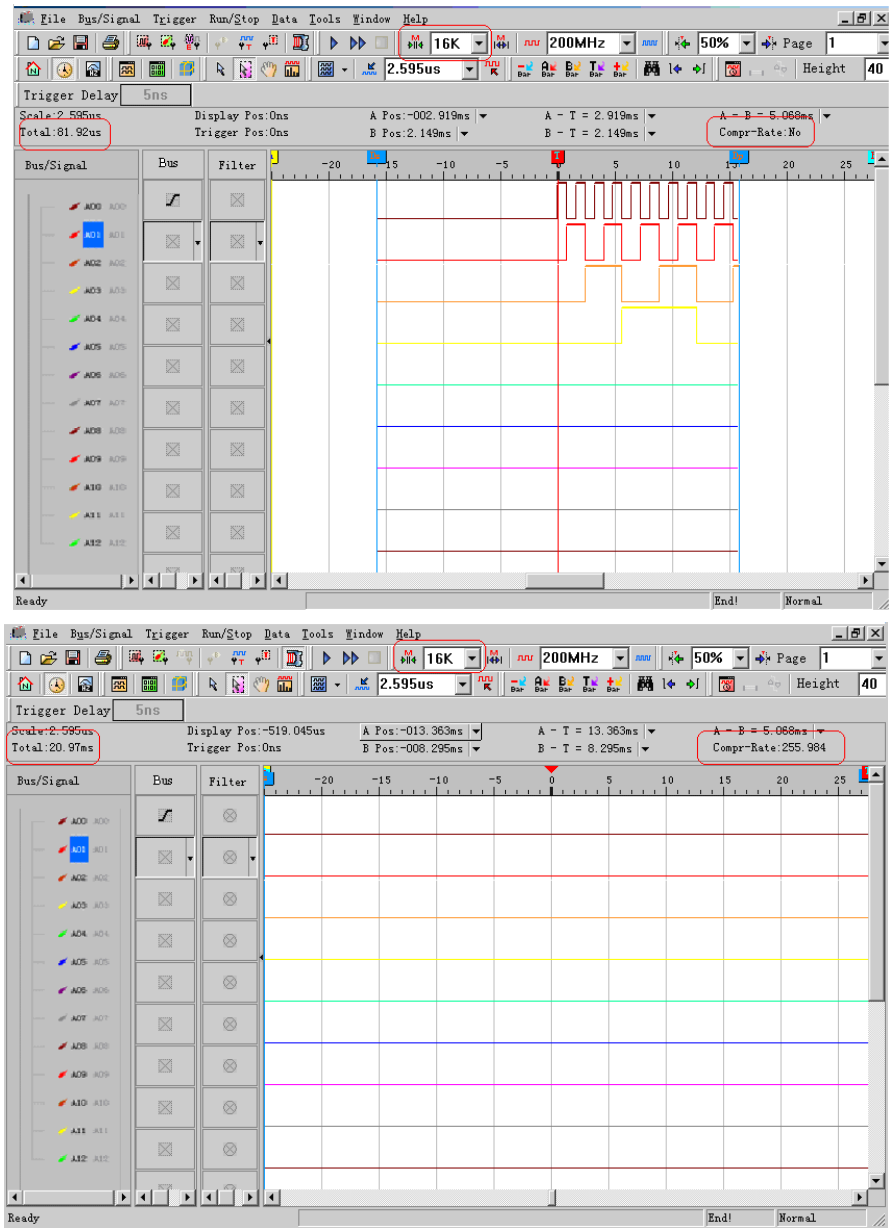


Fig 4-143 – Before and After Compression

Using 16K memory depth, before compression has been applied, the total of the data was 81.92us; after the compression had been applied, the total of the data was 20.97ms. Therefore, the compression rate is 255.984.

Tip: Click icon to view all data, and then select the waveform analysis tools to analyze the waveforms.

Step 5. Click the compression icon again or click off the compression function to stop compression.

Tip: Compression cannot be applied with the Signal Filter function at the same time.

4.7 Signal FIlter and Filter Delay

The function of the Signal Filter and Filter Delay are to allow the system to keep the required waveform, and filter out the waveforms that aren't required.

4.7.1 Basic Setup of Signal Filter and Filter Delay

Software Basic Setup of Signal Filter / Filter Delay

Step 1. Set up RAM Size, Frequency, Trigger Voltage and Trigger Position as described in Section 4.1.

Step 2. Set up the trigger edge on the signal or the bus to be triggered.

Step 3. Click icon, or click the Signal Filter function from the Sampling Setup dialog box and the Signal Filter Setup dialog box will appear.

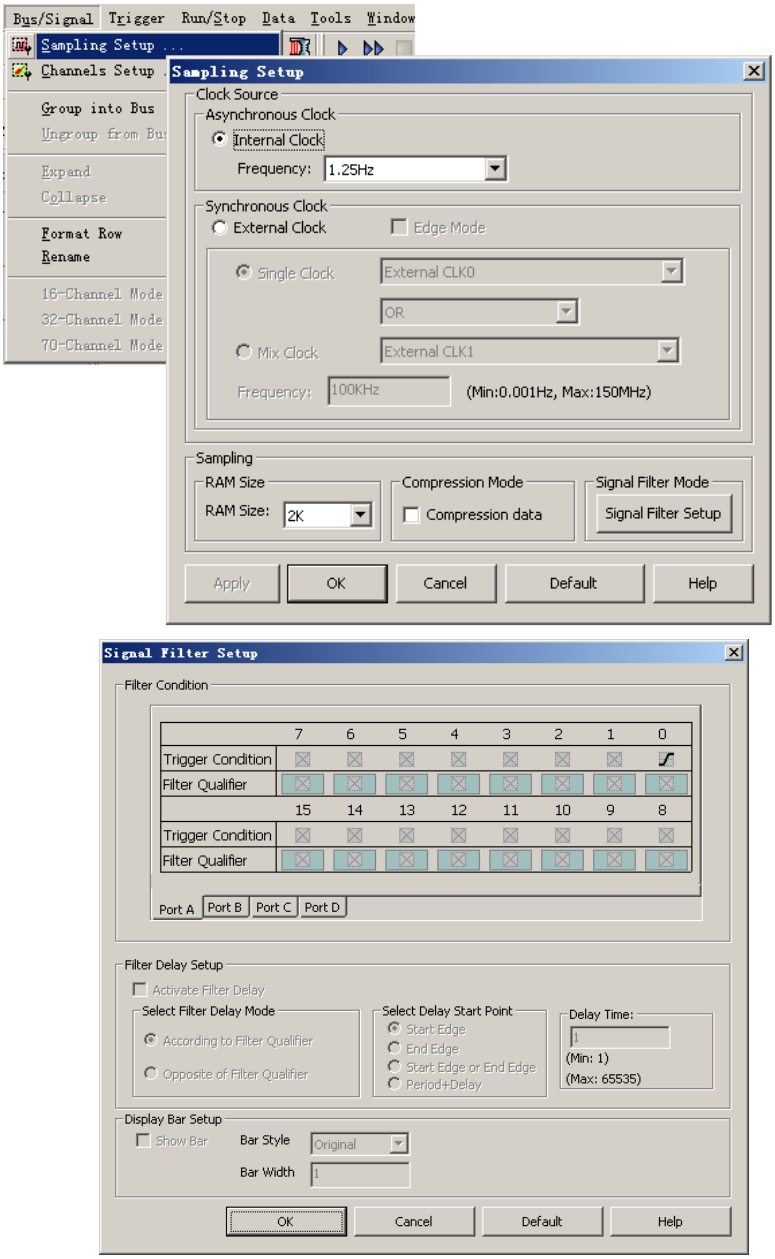


Fig 4-144 – Signal Filter Setup

Step 4. Signal Filter Setup

1. Set up the Filter Qualifier as or on the signal to be analyzed.

2. Click **OK**, then click Run and activate the signal from the tested circuit to the Logic Analyzer.
3. The system will only display the waveforms of the signals which are qualified by the Filter Qualifier.

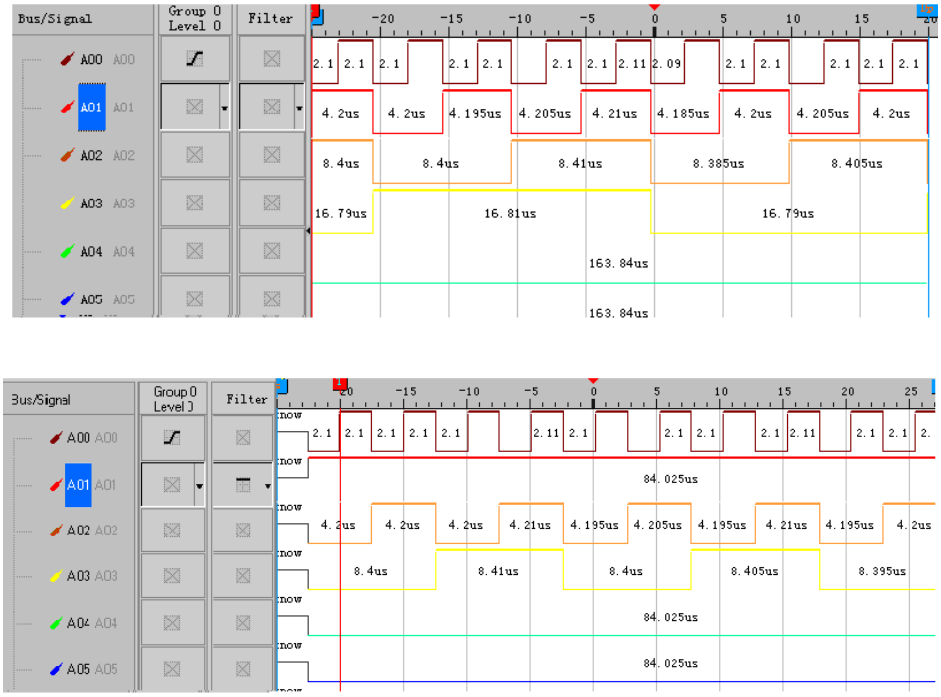


Fig 4-145 – Without/With Signal Filter Setup

The first picture shows the result without Signal Filter setup.

The second picture shows the result which has set the high level on the Filter Qualifier of the signal A01. Only high status of the A01 waveform is displayed.

Step 5. Filter Delay

1. Click on the Filter Delay function as shown in Fig 4-144.
2. Click on the "According to Filter Qualifier" or the "Opposite of Filter Qualifier" functions to select the waveforms to be kept.
3. Click on the "Start Edge" , "End Edge" "Start Edge or End Edge" or "Period + Delay" functions to set the Start Point of Delay.
4. Type the value of the Delay Time into the column of the Delay Time.
5. Click **OK**, then click Run and activate the signal from the tested circuit to the Logic Analyzer.
6. The result will be displayed in the waveform display area as shown in Fig 4-145.

Step 6. Stop Signal Filter/ Filter Delay

Click **Stop**, then click Filter icon and select **Cancel** from the Filter Setup dialog box to stop the Signal Filter or the Filter Delay functions.

Tip: Click **Stop** to check the conditions of the Signal Filter or the Filter Delay setup if there aren't any results.

Tip: Click icon to view all the data, and then select the waveform analysis tools to analyze the waveforms.

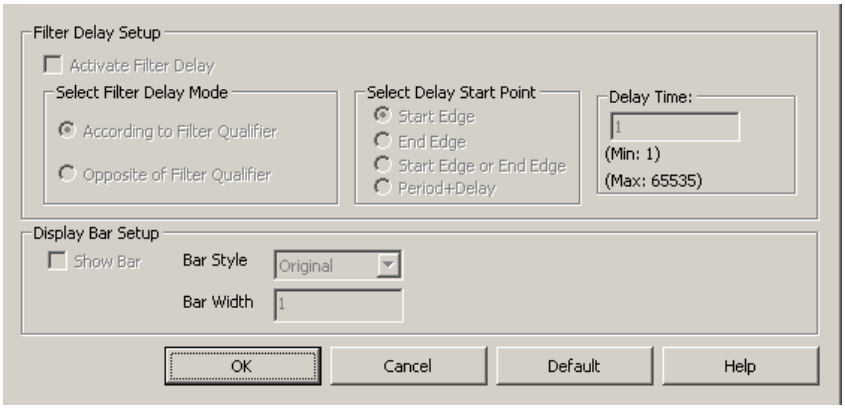


Fig 4-146 – Filter Delay Setup

Tip: Definitions of the Start Edge, the End Edge and the Period + Delay are listed as Figs 4-147, 4-148, 4-149 and 4-150.

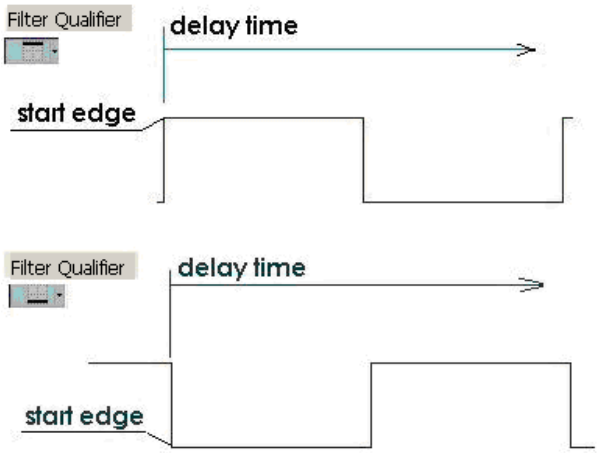


Fig 4-147 – Start Edge

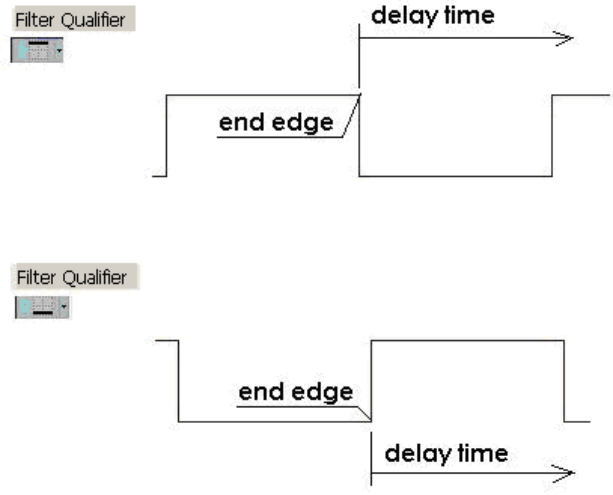


Fig 4-148 – End Edge

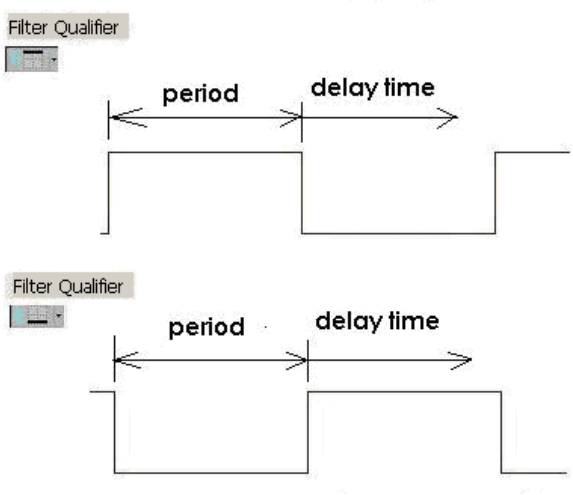


Fig 4-149 – Period and Delay Time

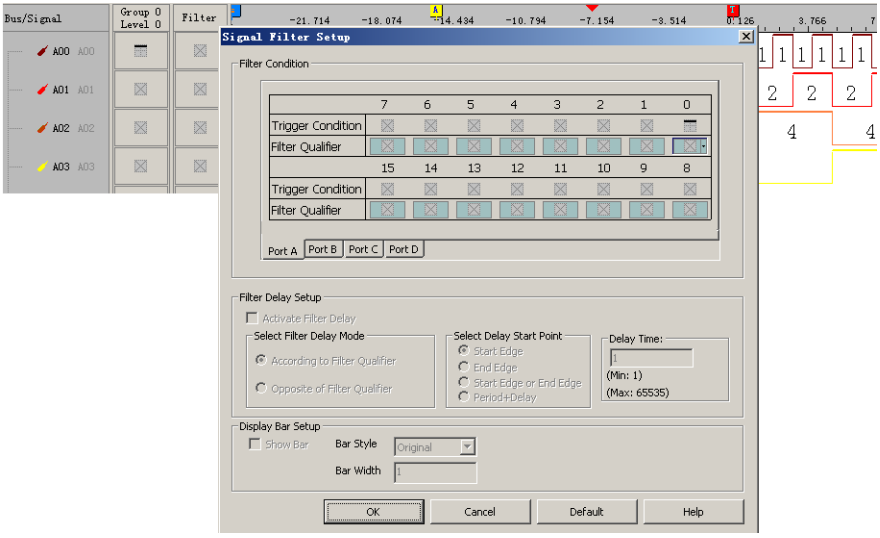


Fig 4-150 – Filter Delay Setup

Step 7. Signal Filter Time Interval

1. Click Display Bar function to know the length of the tested and deleted signal as shown in figure below.

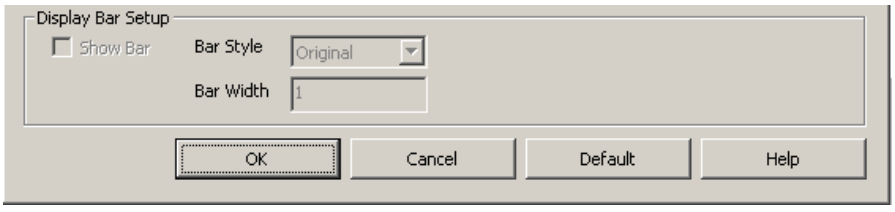


Fig4-151 - Display Bar

2. The bar has two styles which are Original and Bar; the default is Original style which denotes the Display Bar function cannot be used; when selecting Bar style, the Display Bar function can be activated.

3. Bar Width function, when Bar Style is selected, the Bar Width can be set by users.

Tip: The minimum bar width is 1, and the maximum bar width is 65535. If the value exceeds the range, or the font is not according to the requirement, a tip window will appear.

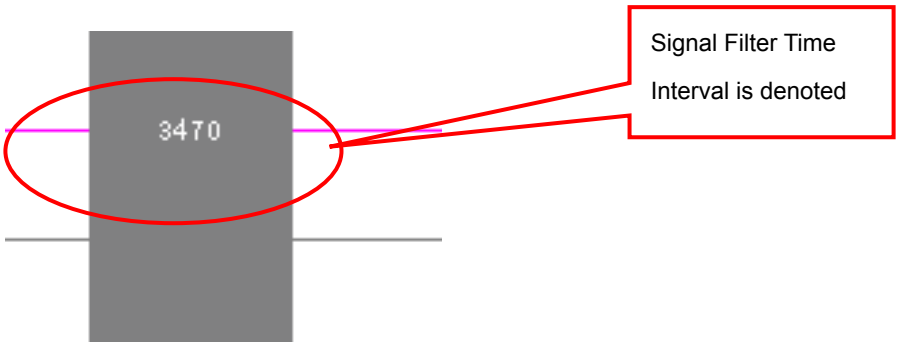


Fig4-152 – Signal Filter Time Interval

Tip: The Signal Filter Time Interval function is limited under the following situations:

A: The Filter Delay Setup and Display Bar Setup are not available under the Compression function.

B: The Filter Delay Setup and Display Bar Setup are not available under the Double function.

C: The final two data are NULL.

D: Logic Analyzer supports the Signal Filter Time Interval function on the condition that the interval between Signal Filter must be more than two clocks.

4.8 Data Contrast

In order to make users analyze data better and contrast the differences of the data, there are adding Data Contrast function. Hereinto, Waveform Contrast is used to contrast the differences between two signals of the same style. One is the basic file; the other is the contrast file. And also the different waveform segments between those two files can be displayed in the contrast file.

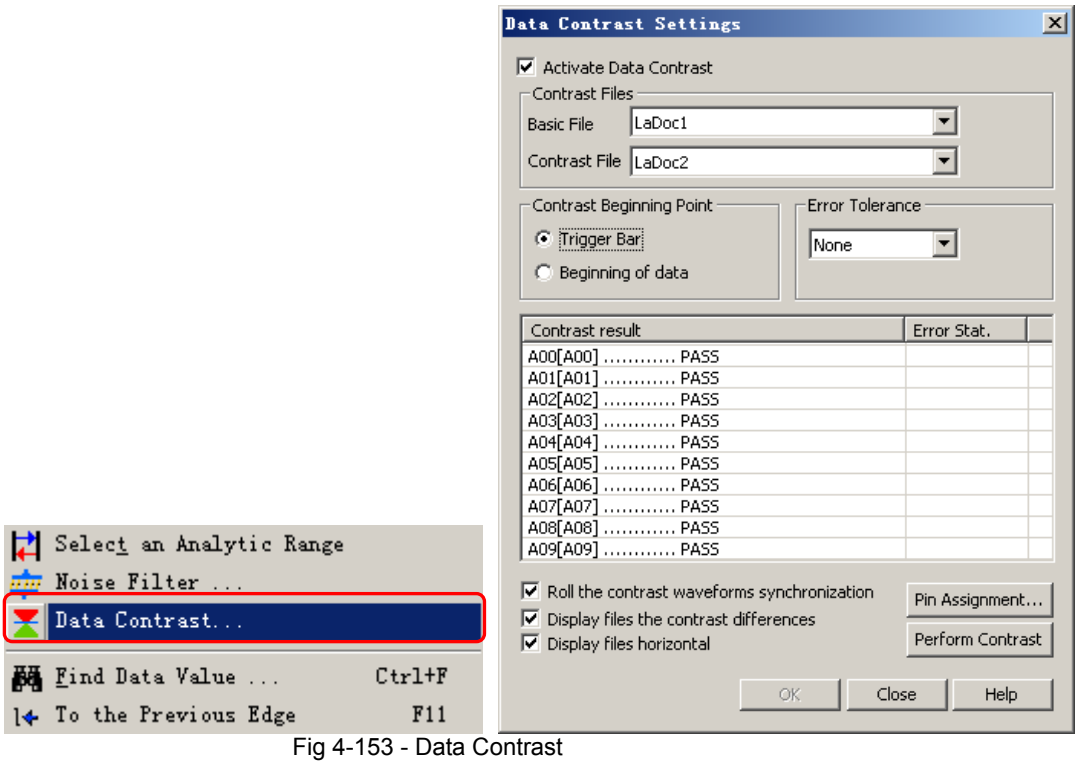


Fig 4-153 - Data Contrast

Activate Data Contrast: Select whether the data contrast function is activated.

Basic File: The basic file is used as a standard contrast file.

Contrast File: The file is used for contrasting with the basic file.

Contrast Beginning Point: It is used for setting the contrast start point.

Trigger Bar means the files are started to contrast at the position of T Bar.

Beginning of data means the files are started to contrast at the beginning of the data.

Error Tolerance: Set the allowed range value when the two waveform files are being contrasted; the value can be set as None, 1 clock, 2 clock, 3 clock, 4 clock, 5 clock, 6 clock, 7 clock, 8 clock, 9 clock and 10 clock, and the default is None. If the error tolerance is set as 2 clocks, the differences within 2 clocks won't be marked and the error statistics won't include the differences within 2 clocks .

Error Stat.: It is used to show the number of the differences between the basic file and the contrast file.

Display files horizontal: When the function is activated, the contrast files can be displayed horizontally. Users can decide whether activate this function or not, and the default is not activated.

Roll the contrast waveform synchronization: When the function is activated, the contrast files can be rolled synchronously. Users can decide whether activate this function or not, and the default is not activated.

Display files the contrast differences: When the function is activated, the different waveform segments can be marked in the contrast waveform. Users can decide whether activate this function or not, and the default is not activated.

Pin Assignment: Select the channel that needs to be contrasted.

Perform Contrast: Click this button, then the software starts the data contrast immediately.

The Function of Finding Contrast Results

In the tool column, we add the function of finding contrast results in the tool bar, which is used to display the differences of the two waveform channels much clearer when contrasting the two waveform files.

Users can't use the function of finding contrast results unless they have selected the contrast file, or the two labels are displayed in gray. It is noticed that the function of the finding contrast results is only used to find the contrasted results of the channels which are required in the contrast file, at the same time, the found waveform differences will be displayed in the center position of the waveform area. The function of finding contrast results cannot work when the Bus is selected as the contrast file.

Image Interface:

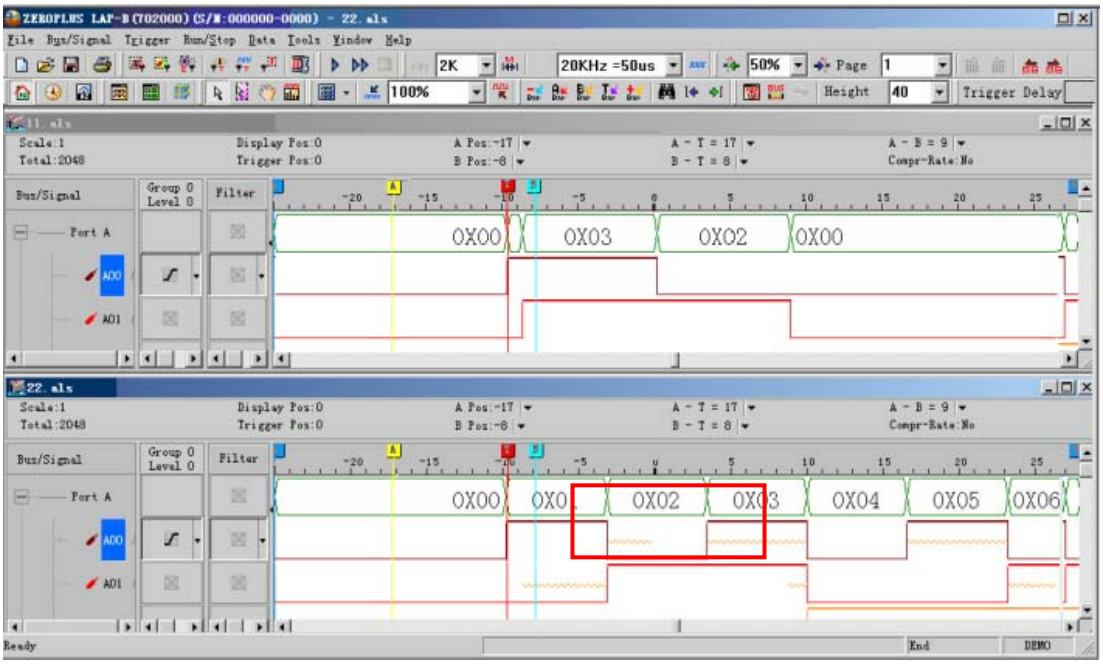
Fig 4-154 – Tool Bar

The former data contrast : Select the channel in the contrast file, and then click the button to find the former data contrast, as a result, the contrasted result is displayed in the center position of the waveform area.

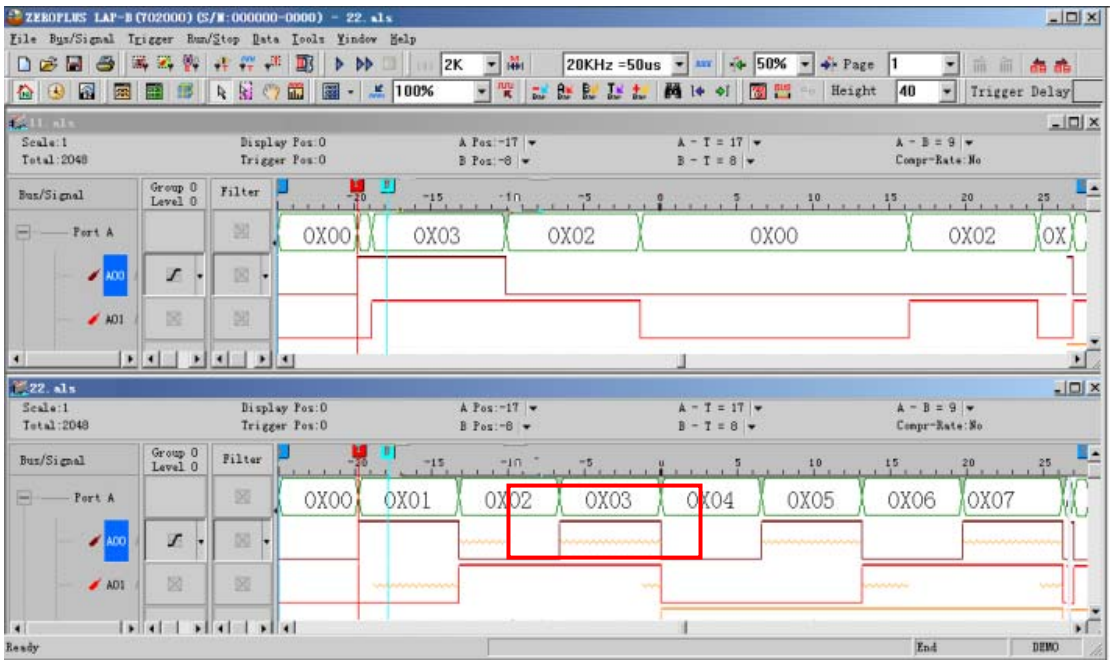
The next data contrast : Select the channel in the contrast file, and then click the button to find the next data contrast, at last, the contrasted result is displayed in the center position of the waveform area.

Operating Instructions:

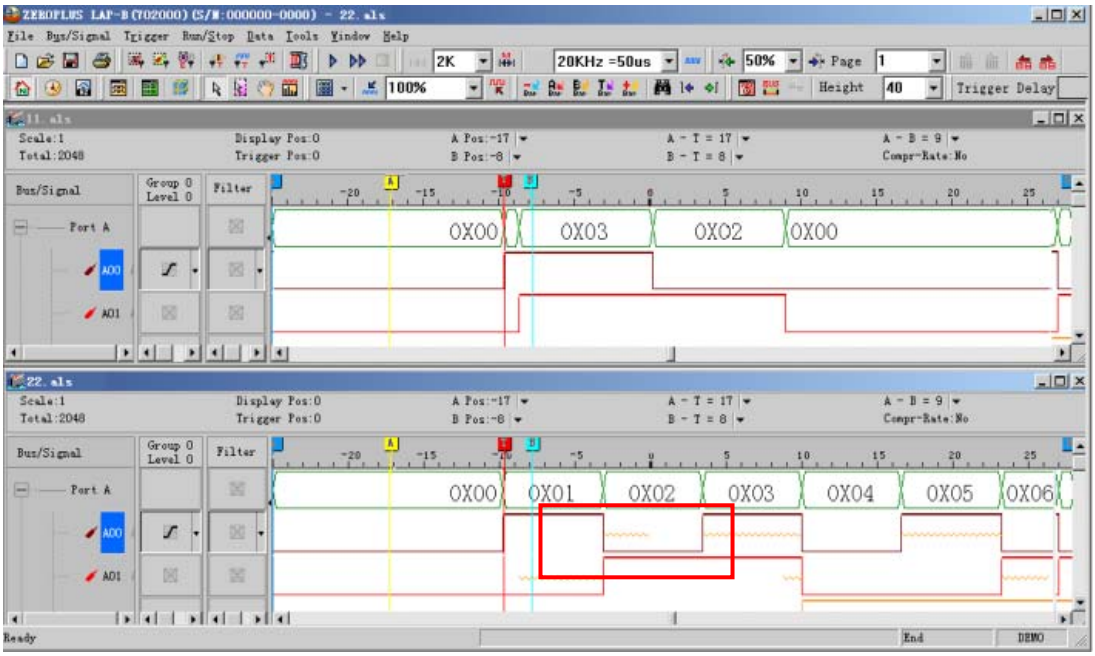
(1) Select the channel A00 in the contrast file to find the differences (the first difference is displayed in the center of the waveform area). See the below image:



(2) Click **the next data contrast** button ; The second difference will be displayed in the center of the waveform area as the image below:



(3) Click **the former data contrast** button ; The first difference will return to the center of the wave form area as the image below:



Data Contrast Mode

1. Display the result of Data Contrast in the data contrast dialog box

After activating the data contrast, the contrast result can be displayed in the contrast result list as the following section in the red frame. The information is very simple. It is not necessary for users to learn more details; users can only know whether the signal of one contrasted channel is absolutely the same to that of the other.

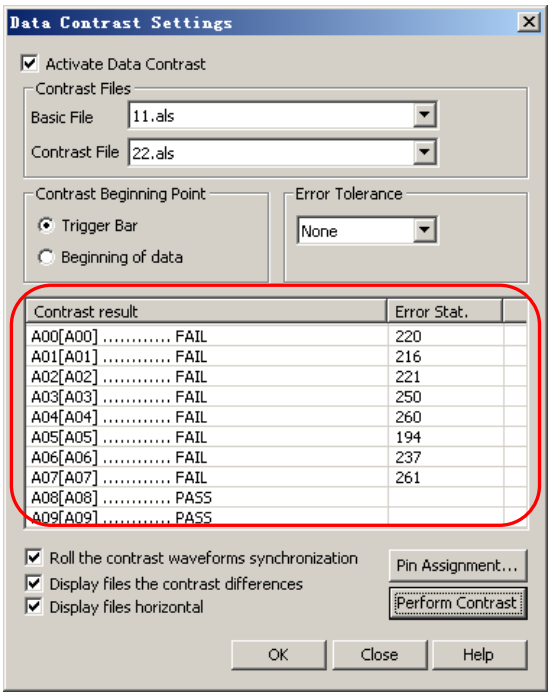


Fig 4-155 - The Result of the Data Contrast Dialog Box

A00[A00] ……FAIL: It denotes that there are differences between the two channels of the two files.

A08[A08] ……PASS: It denotes that the data between the channels of the two files are absolutely the same.

2. Contrast the waveforms in the waveform window

The software contrasts the two data files in the waveform area window, and displays the contrast waveform and

basic waveform horizontally; and users can contrast the two waveform files by rolling the mouse, however, the differences can be marked in red waveform line"~~~~~~~~~".

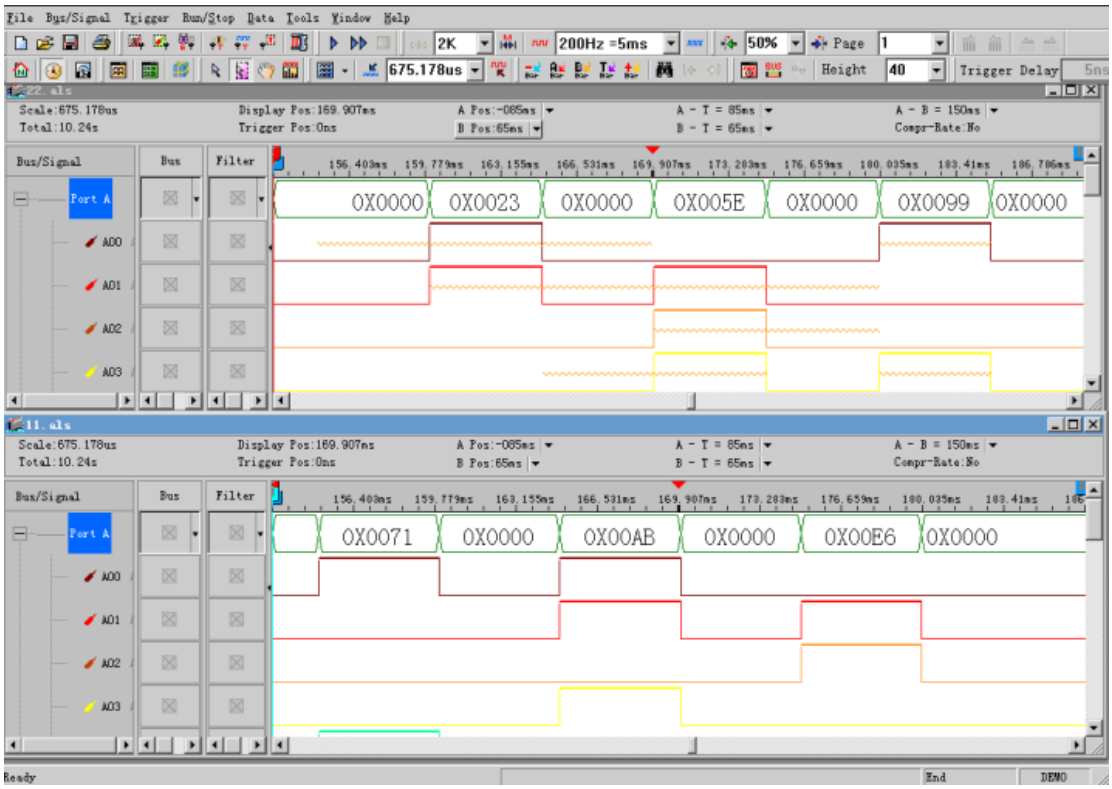


Fig 4-156 - Waveform Window

Note: "~~~~~~~~~" is used for marking the different areas in this contrast file.

4.9 Noise Filter

The Noise Filter function can make the system filter the waveform that doesn't meet users' requirements.

4.9.1 Basic Software Setup of Noise Filter

STEP1. Click **Data** on the Menu Bar, then select Noise Filter to activate the Noise Filter function as the figure below.

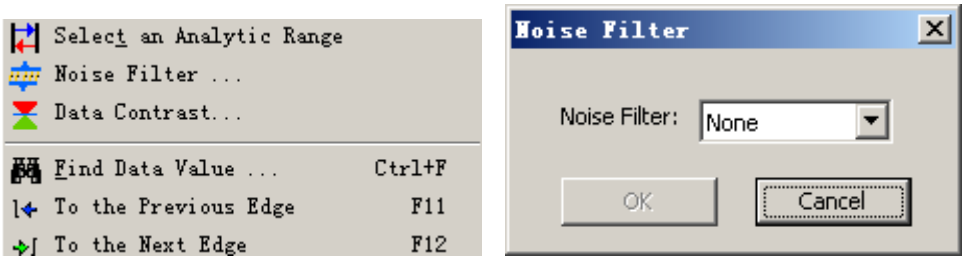


Fig4-157 - Noise Filter

STEP 2.Transmit the tested signal to the Logic Analyzer as the figure below.

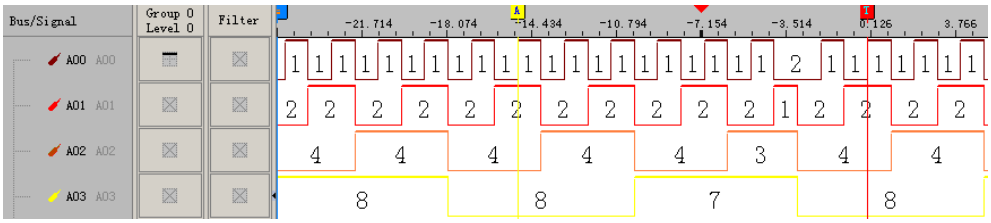


Fig4-158 - Tested Signal

STEP 3.Filter the waveform that are not bigger than 5 clocks.

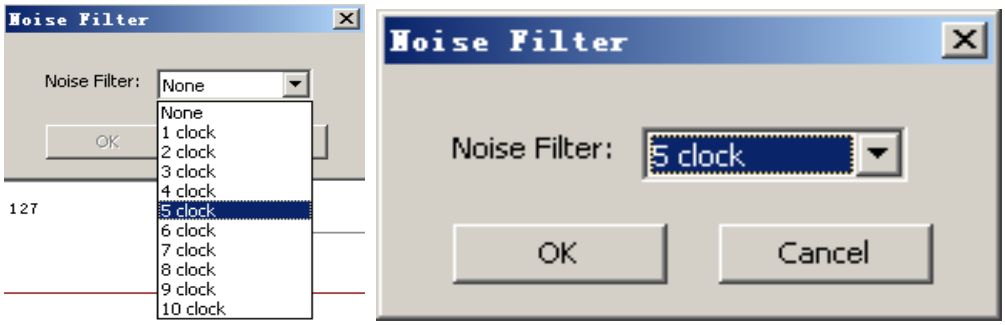


Fig4-159 - The condition of Noise Filter is 5clock.

STEP 4.After filtering the waveform that are not bigger than 5 clocks, the unqualified waveforms are deleted.

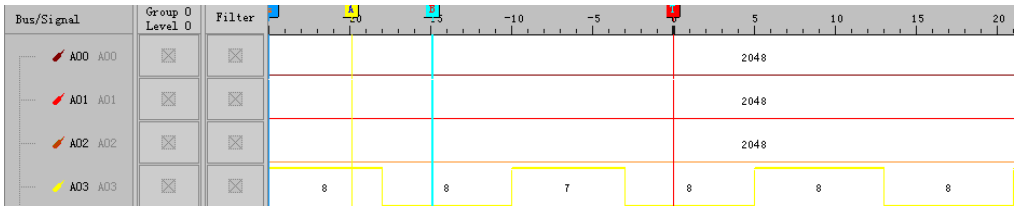


Fig4-160 - Signal after Filtering

STEP 5.Reserve the original waveform: open the Noise Filter window, and then select **None**, the waveform will be restored.

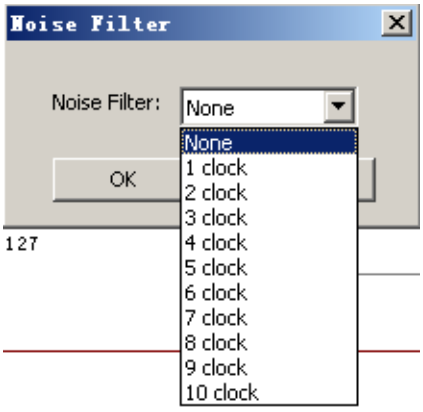


Fig4-161 - Restore the Waveform

4.10 Refresh Protocol Analyzer

The Refresh Protocol Analyzer function can make the system analyze the data between Ds and Dp again.

4.10.1 Basic Software Setup of Refresh Protocol Analyzer

STEP 1.Click **Tools** on the Menu Bar, then select or click on the Tool Bar directly to refresh Protocol Analyzer.

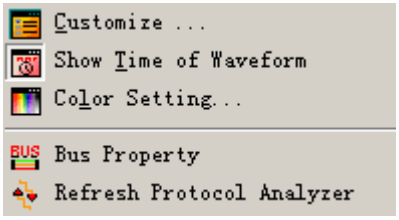


Fig4-162 - Refresh Protocol Analyzer

STEP 2.Transmit the tested Protocol Analyzer signal to the Logic Analyzer, for example Protocol Analyzer SPI.

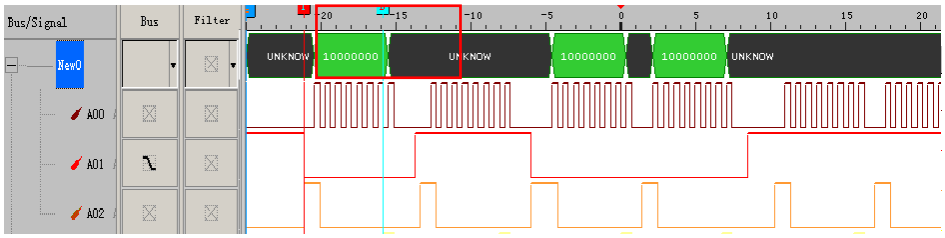


Fig4-163 - Waveform before Refreshing

STEP 3.Choose "Select an Analytic Range" function to select the analysis range, and drag Ds Bar to B Bar.

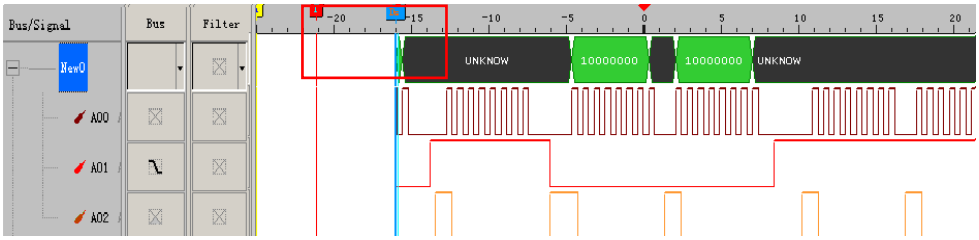


Fig4-164 - Drag Ds Bar to B Bar

STEP 4. Click , the Logic Analyzer will analyze the data between Ds and Dp.

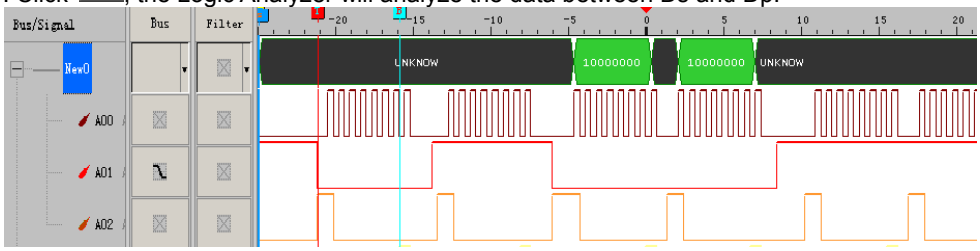


Fig4-165 - Analyze the Data Between Ds and Dp

STEP 5.Click again, the waveform returns to the original state.

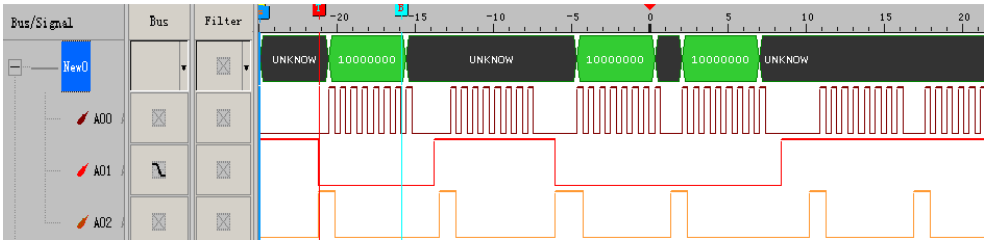


Fig4-166 - Restore the Original State

Tip: The Refresh Protocol Analyzer function has effected, while the Ds and Dp are activated.

5 Troubleshooting

5.1 Installation Troubleshooting
5.2 Software Troubleshooting
5.3 Hardware Troubleshooting

Objective

In this chapter, troubleshooting is divided into installation, software and hardware issues. These troubleshooting questions and answers depend not only on our engineers, but also on end users such as students, engineers, technical manual writers, and others.

5.1 Installation Troubleshooting

Q1. Why is there no prompt when I insert the driver CD into my CD-ROM?

A: At this stage, the driver CD is not auto-executable. The primary issue here is a chipset problem. Though these four Logic Analyzer models seem only different in model number, they are quite different in firmware and chipsets. Due to installation procedures (see *Chapter 2*), we are unable to compile a driver program that auto-detects the chipset at the beginning of the installation.

Q2. Why does the installation software keep giving an error message saying that I don't have enough memory?

A: This kind of problem happens in many hardware installations. Turning off multimedia programs such as Media Player, media decoders, media encoders, and so on. If there are any multimedia icons in the system tray (see the far right end of the **START** menu taskbar), remove them. The Logic Analyzer software will run better in memory locations from 64 to 512 MB.

Q3. What if I want to share this software interface with all users of my computer after installing it?

A: The shortcut is removing the software interface ,and then reinstalling it. By default, the program is available for all users.

Q4. My HDD is modest; which software components are absolutely necessary?

A: Choose **Custom** as your setup type. Next, unselect items such as examples and tutorials. You must install at least the Main App (application).

Q5. My MS Windows system will not accept the driver; what can I do?

A: Double check that you run the correct Setup.exe from the folder that corresponds to your hardware and MS Windows version. Visit our website for the latest updated or debugged software. If you are running this program on a virtual machine, the virtual machine may not support the amount of hardware addressing. In this case, try it with a machine that is physically running a Windows system.

5.2 Software Troubleshooting

Q1. Can I run the program even if I don't have the Logic Analyzer hardware?

A: Yes, you can. You can run the program under the demo mode. See. *Fig5-1*.

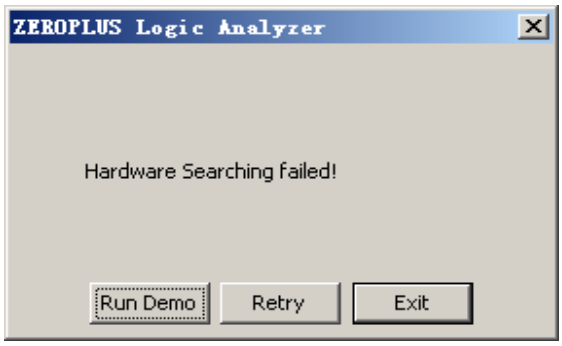


Fig. 5-1: Select **Run Demo** if you do not have the actual hardware.

Q2. I am running a graphing program and software at the same time. Whenever I try to make a screenshot of my work, it keeps telling me that I have insufficient memory space; what is wrong?

A: A few users have reported similar problems. We are not certain what causes it or how to fix it. However, we have found that if there is a defective address within 128 MB to 512 MB in your physical memory, your software might signal "End of memory". Thus, the program will warn you about insufficient memory. Test your memory with a varied memory testing program. Or, take a screenshot, close the program, paste it to the graphing program, and re-open the program.

Q3. A part of the background picture remains within the Position Display Area, especially when running the program in Demo Mode. What's wrong with it?

A: Your machine may have a memory management problem with either your physical RAM onboard or the RAM on your video card. Turn off any other multimedia of graphic programs and then re-run the software. If this does not work, restart your system. This should temporarily fix the problem. However, we highly recommend terminating all irrelevant programs while working with the Logic Analyzer (Try not to burn DVDs, listen to music or watch movies while working with the Logic Analyzer.).

Q4. The default color setting of the Position Display Area is very cool, but I don't see anything when I print my work out with my black and white laser printer. What can I do?

A: Refer to *Section 3.6*; it should have clear, understandable instructions about changing the color of the user interface. See *Fig. 3-136*; this color setting should give a clear view of the Position Display Area, even with an old black and white laser printer.

5.3 Hardware Troubleshooting

Q1. Why are no lights on when I hook the USB cable to the Logic Analyzer?

A: Double check whether the other end is properly connected to your PC. There may also be a defect in your USB cable. Try another cable.

Q2. Why can't I read any signals from my Logic Analyzer?

A: Check whether you have correctly connected the signal cables to the activated pin on your test board and check the power supply of your test board. The Logic Analyzer does not supply any electricity to a test board via signal lines.

Q3. I get a signal from only one Logic Analyzer when I have two connected; what is wrong?

A: Currently, only the LAP-B(702000) supports many Logic Analyzers working in series. Also, make sure that the signal lines, power lines, and ground line are properly connected. Refer to Fig*. 1-11, Table 1-2, Table 1-3, Table 1-4*, and *Table 1-5*.

Q4. Why should I bother grounding? Where can I ground?

A: Grounding will protect the Logic Analyzer and the test board. A proper ground may improve the quality and accuracy of your data. Since it is impossible to avoid unwanted interference you may ground the Logic Analyzer with the test board to ensure that unwanted interference will equally disturb both the testing and tested devices, ensuring a set of data that is still accurate.

Conclusion

Every user of our product is a potential writer for *Chapters 5~7* in this User Manual. In fact, this chapter is a composition of many unnamed electronic professionals, especially experts.

6 FAQ

6.1 Hardware
6.2 Software
6.3 Registration
6.4 Technical Information
6.5 Others

Objective

In this chapter, common problems and questions are roughly classified into five categories: Hardware, Software, Registration, Technical Information, and Others. This is a backup resource for users, especially those without Internet access. Most references refer to English web links.

6.1 Hardware

H01. Is it ok to substitute stock items for bundled cables and connectors?

A: Yes, users may use any compatible connectors and cables. However, to ensure consistency and accuracy in measurements and data, we strongly recommend using the bundled connectors and cables. Each of the Logic Analyzer is calibrated with the bundled cables and connectors before packing.

H02. Does Zeroplus manufacture grippers? How may I purchase grippers?

A: Yes, we have a production line dedicated to grippers. Contact our sales department and a sales representative will be happy to assist you.

H03. Is the memory size fixed? If I just use one of the ports, can I expand the memory size?

A: The Logic Analyzer's memory is fixed at 4 megabits. Due to current hardware limitations, the memory size cannot be modified, even as the number of ports used change.

H04. Are different external sampling frequencies for different channels possible?

A: No, there is only one external sampling frequency available.

H05. Can I disable or set a certain port to *don't care* while during compression?

A: No, during compression, D Port will be set to be **disabled**.

H06. Why does the Logic Analyzer feature negative voltage calibration?

A: This allows users to analyze any given signal.

H07. How do I adjust the Trigger Level?

A: The adjustment of the trigger level is done with a port which consists of 8 channels. The trigger leveL can only be adjusted for an entire port.

H08. Does the Logic Analyzer use hardware or software compression technology?

A: For time efficiency, the Logic Analyzer uses hardware compression.

H09. Is planning an Analyzer that can handle more channels?

A: Yes, we are working in this direction.

H10. Does the memory page vary when the depth of the memory changes?

A: Yes, the depth of memory changes the memory page.

H11. Is the Logic Analyzer expandable? How may I expand it?

A: Yes, the Logic Analyzer is expandable. At this stage, you can expand it with external module devices.

H12. Why must I reinstall the driver every time I use a different the Logic Analyzer?

A: Since each Logic Analyzer has unique serial numbers, you must reinstall the driver every time you change the Logic Analyzer.

H13. Why is there no data? Why does data sampling seem inconsistent?

A: The reasons are varied, but you may follow this checklist for troubleshooting:

1) Always check the USB connection between the Logic Analyzer and your PC.
2) We strongly recommend using USB ports in the rear panel of a PC; these ports usually have better voltage stabilities than front panel ports. However, if front panel USB ports are directly soldered to the main board, you can use them.
3) Make sure the Logic Analyzer is directly connected with the PC (without a USB hub).
4) Inconsistent data display may indicate voltage irregularities in the main board; examine capacitors on your

main board or power supply.

5) If the problem is the power supply, we strongly recommend purchasing a power supply with a hardwired voltage transformer rather than a voltage regulator. For power supplies with the same output power, those built with hardwired voltage transformers are usually much more heavier than those relying on voltage regulators.

H14. What are the time settings for "Setup" and "Hold"?

A: Setup Time: 0.05ns ~ 0.25ns; Hold Time: 0.02ns ~ 0.08ns.
Clock High requires a minimum of 0.31ns. **Clock Low** requires at least 0.47ns.

6.2 Software

SW01. Why is the compression function not activated by default?

A: Mostly to avoid significant errors when testing signals with high variability, or measuring a certain channel for a long time period.

SW02. What is the purpose of the Compression Function?

A: The Compression Function measures signals that vary slightly over a long period.

SW03. Can I activate the Trigger Page and Compression Function simultaneously?

A: Yes, you can.

SW04. When should I use the "Bar" function?

A: This function allows you to highlight a segment of a waveform so that you can have a closer view. Depend on the configuration of **Position Display Area Data Mode** under **Tools ➔ Customize**, a more accurate numeric value of address, time, or frequency difference will be calculated and displayed as shown in *Fig. 6-1*.

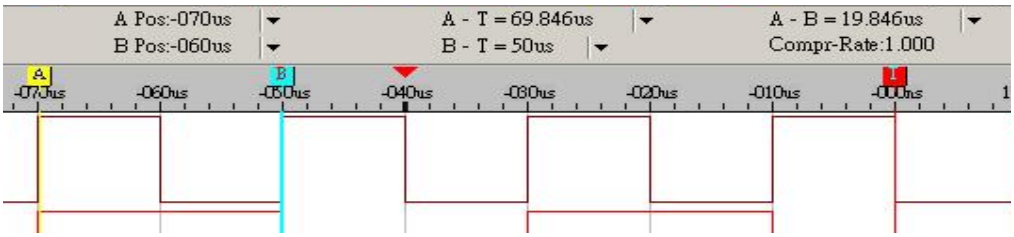


Fig. 6-1 – Bar Function

SW05. Can triggers be differentiated in Pre-Trigger and Post-Trigger?

A: Yes, they can.

SW06. Are all setup parameters and configurations saved as I save my work?

A: Yes, everything in your work space, except signal graph, will be saved.

SW07. If I have the wheel feature with my mouse (or other pointing devices), may I adjust the waveform display zoom, in the Position Display Area by scrolling?

A: This feature has been enhanced since V. 1.03. If your program version is prior to this version, visit our website for the latest update at
http://www.zeroplus.com.tw/new_instrument/main-download.php?type=1

SW08. What are the extremes for Delay Time and Clock & Trigger Delay Clock?

A: The interface will inform you of the interval you may use. However, it varies from case to case, depend on your test devices. See *Fig. 6-2*.

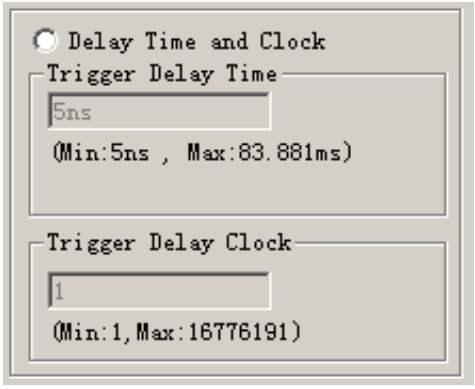


Fig. 6-2 – Delay Time and Clock

SW09. How do I know the version number of my software interface program?

A: Click **Help** from the Menu Bar *(See Fig 6-3)*,
and then select **About ZEROPLUS Logic Analyzer**(*See Figs 6-3 and 6-4)***.**

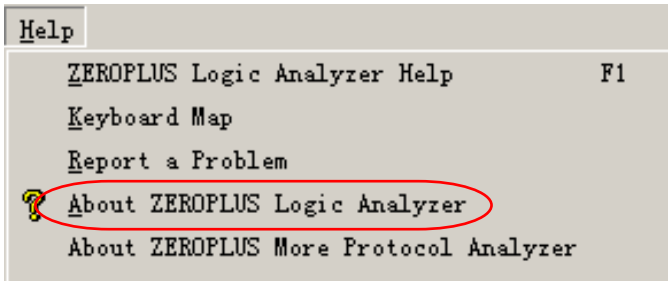


Fig. 6-3 – About ZEROPLUS Logic Analyzer

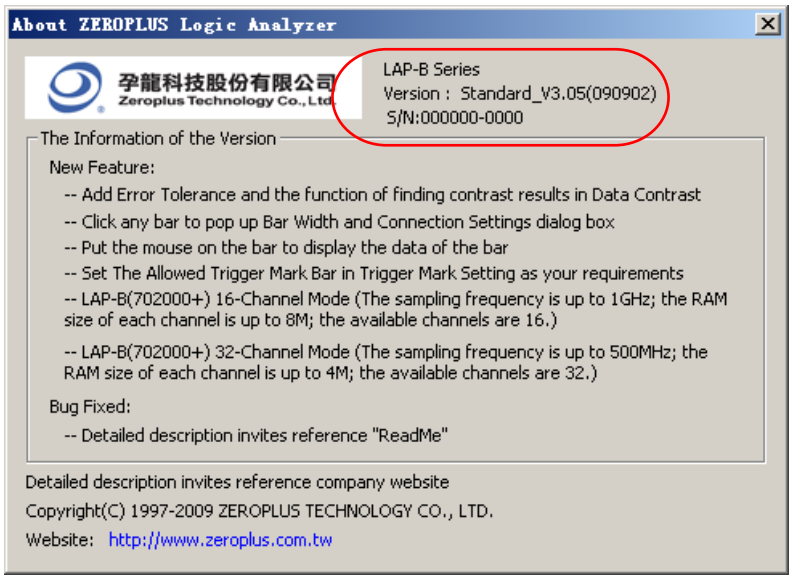


Fig. 6-4 - The circled information is the version number.

SW10. How may I upgrade my software interface program?

A: Visit our website at http://www.zeroplus.com.tw and follow the instructions for the English version. You may also use the following address for English updates: http://www.zeroplus.com.tw/new_instrument/main-download.php?type=1

SW11. Can I save my signal data to a separate pure text file (*.txt)?

A: Yes, this feature has been available since V1.03.01.

SW12. Why is the text display covered by other text or outside the display width?

A: At this stage, our software interface program has missing code for multilingual support. You will have to ensure your system default encoding is one of the following languages: 1) any English Encoding (en, en-XX), 2) Traditional Chinese (zh, zh-XX), 3) Simplified Chinese (zh, zh-CN in HZ, GB2312, GB18030). Double check the language configuration in **Regional and Language Options**.

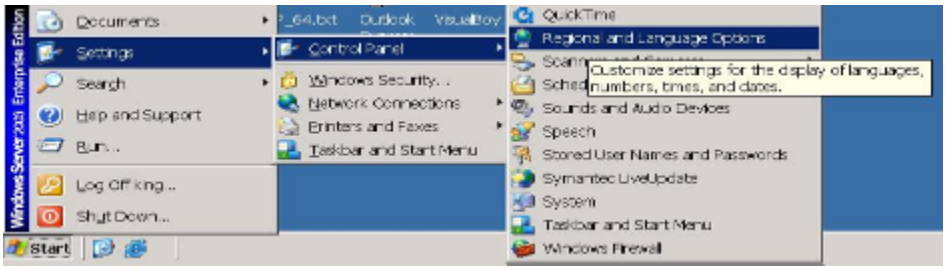


Fig.6-5 – Windows Regional and Language Options

SW13. Is there a Reset that restores the default color setting for signal output wave forms in the Position Signal Display Area?

A: Yes, there is. Click **Tools** from the Menu Bar, and select **Color Setting**; click **Default**. However, this restores everything in this window. You must make a further adjustment if the color setting is the only thing you want to restore. *See Fig. 6-6.*

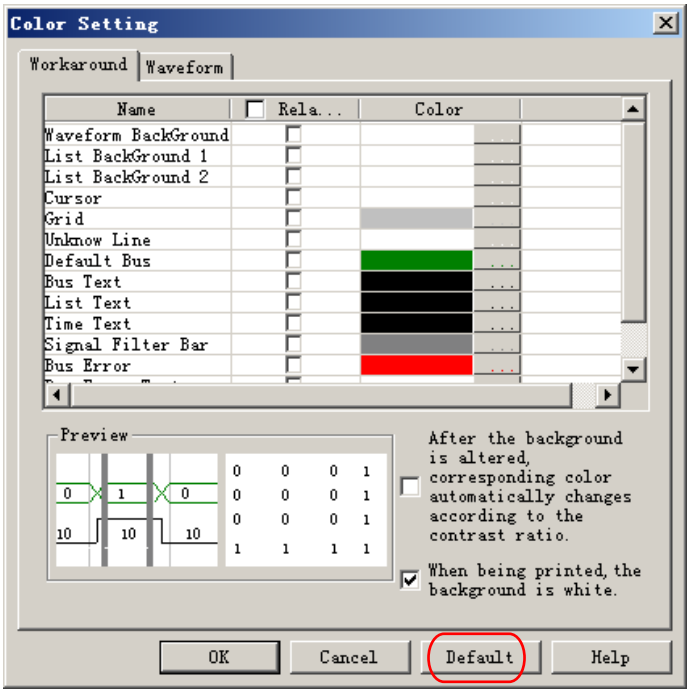


Fig. 6-6 – Restore Color Default

SW14. Can I change the displayed waveform mode?

A: Yes, you can. There are two ways to do this.
First, go through **Data ➔ Waveform Mode** and choose a waveform. *See Fig. 6-7.*

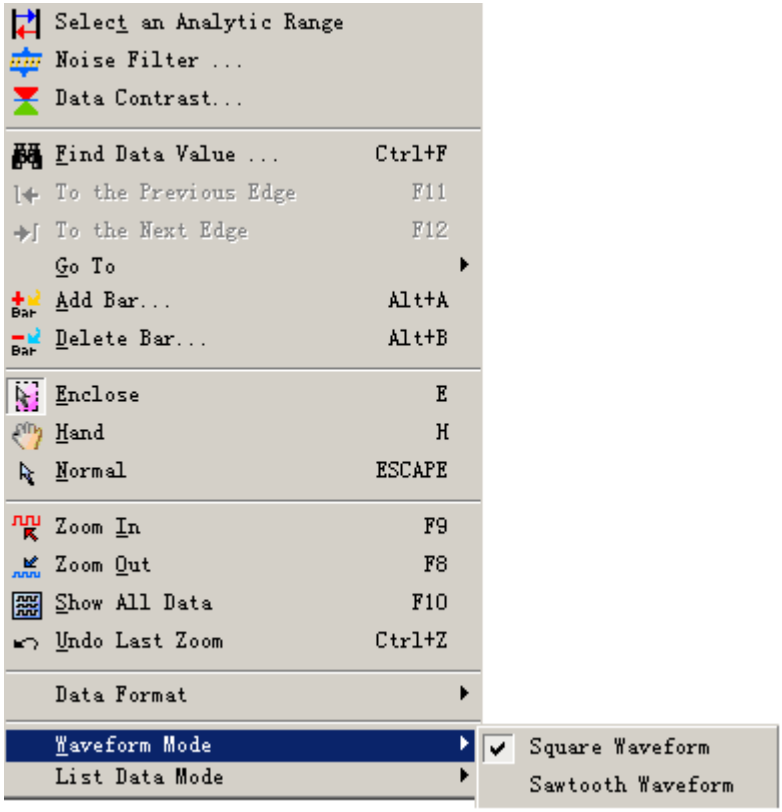


Fig. 6-7 – Waveform Mode (1)

The second alternative is to right-click any place in the Waveform Display Area. This will pull out a menu. Click **Waveform Mode**, and choose a waveform. *See Fig. 6-8.*

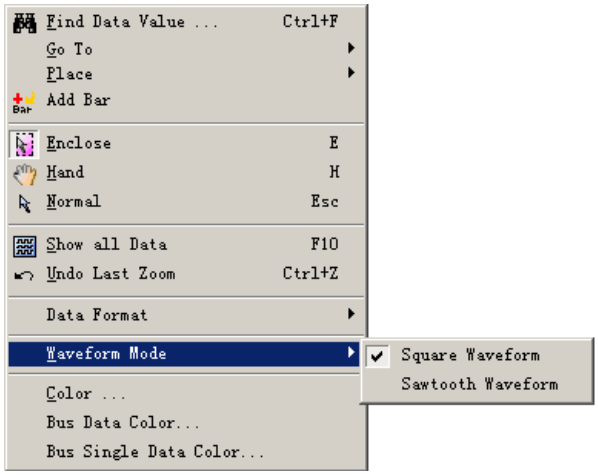


Fig.6-8 – Waveform Mode (2)

SW15. Can I change the Signal Display Mode into the Timing mode?

A: Yes, you can.

SW16. Why does Filter Delay not work when the Double Mode is activated?

A: To optimize signal output quality and maximize memory efficiency, the **Signal Filter** function may work under the Double Mode. However, the **Filter Delay** function DOES NOT work under the Double Mode at this stage.

6.3 Registration

RG01. What is the significance of the hardware serial number?

A: Every product is assigned and engraved with a unique serial number, which allows us to trace the original manufacturing date of a specific product.

RG02. How do I register online?

A: Visit our homepage at http://www.zeroplus.com.tw. Choose the Instrument Department, and click on **English**. You may also enter the following address:
http://www.zeroplus.com.tw/new_instrument/main-member-register.php?flag=insert
Once you finish membership registration, proceed with product registration. After finishing product registration, you will receive an email consisting of your product registration information. A password may be required for further customer services and other inquiries.

RG03. What should I do if online registration fails?

A: Do a screen grab of the window, including the error message, and email our customer service department. A customer service representative will be glad to assist you as soon as possible, once the email is correctly received.

RG04. How may I register if the purchasing date was longer than one month?

A: In this case, fill in the registration card and send it via post, fax, or email to our customer service department, and a representative will process the registration for you.

RG05. What is the warranty length for my product?

A: A two-year FACTORY WARRANTY is offered in which you will have to send the defective product to the closest branch, an authorized service site, or our headquarters. The in-store warranty may vary, and many require extra charges for various extended warranty policies. The company is not being responsible for an in-store warranty that exceeds our factory warranty.

RG06. Why should I register this product?

A: If you do not register this product, the warranty will be counted from the manufacturing date indicated by the serial number of your product. Thus, we strongly recommend registering your product, for your own benefit.

RG07. What should I do if the hardware serial number is previously registered?

A: In this case, take a picture of the decal on the rear side of the product and fill in the registration form. Call us and mail both picture and registration to us. A customer representative will be happy to assist you.

RG08. How do I register my protocol analyzer and buy protocols?

A: Every product is assigned and engraved with a unique serial number. Please print your S/N number window as an example attachment and send it to your distributor or ZEROPLUS head office. According to your S/N, we will provide passwords for your protocol registration.

6.4 Technical Information

TI01. What is the Logic Analyzer?

A: The Logic Analyzer is a tool that sieves out and shows the digital signal from a test equipment by using a clock pulse. The Logic Analyzer is like a digital oscilloscope. However, it only shows two voltage states (the logic status 1 and 0), differ from many voltage levels of an oscilloscope. The Logic Analyzer has more channels than an oscilloscope to analyze the waveform. Since the Logic Analyzer obtains only signals 1 and 0, its sampling frequency is slower than an oscilloscope, which needs many voltage ranks. Moreover, the Logic Analyzer can receive many signals during a test.

TI02. How does the Logic Analyzer operate?

A: The Logic Analyzer reserves trigger requirement setting for users and uses them on the test equipment for the value of the sampling signals and puts them into the internal memory. The software of the Logic Analyzer will read out the value from the memory and switch it to the waveform or status shown for users' analysis.

TI03. What is the asynchronous Timing Mode?

A: Since the sampling clock and tested objects are not directly related to each other, and the former won't be controlled by the latter, the sampling clock and the tested signals will not be done at the same time. We call this "Timing Mode", which means that in the same time interval, you can get sampling data from the test equipment at one time, such as every 10 seconds. The internal clock, the Logic Analyzer's inner confirmed one, is often for sampling in Timing Mode as is the logic waveform.

TI04. What is the synchronous State Mode?

A: Because the sampling clock and measured object can be directly related, and are controlled by the latter, signals of the former and the latter can proceed simultaneously. We call this "State Mode". In this mode, the measured object provides the sampling clock. State Mode is that the Logic Analyzer can obtain sampling data from the test equipment synchronously. In other words, when the test equipment has a signal or signal group, it is the time to get the signal. For example, while the test equipment is sending out one rising edge, the Logic Analyzer can start to obtain one signal.

TI05. What are A-bar, B-bar and T-bar?

A: The T-bar, A-bar and B-bar are labels. T is the trigger label, which cannot be removed when the waveform or the state is displayed, which marks a pod. When searching for, or obtaining data, the A and B labels can be set in any location. Use the order of these markings, you can return quickly to the desired position to analyze data. This can also be a point to measure the interval among A-B, A-T, and B-T.

TI06. What is a Trigger Gripper?

A: A gripper is the gathering point to collect the Logic Analyzer channels. When a cable connector is not suitable for the tested device, a trigger gripper may be an alternative for connection.

TI07. What is a Channel?

A: The channel is the collection line of the input signal. Each channel is responsible for linking the pin of the measured device. Every channel is used to collect signals from the test equipment.

TI08. How can I display acquisition in the waveform captured by external sampling signal?

A: Select **waveform Display** from the **Window** list.

TI09. What is an External Trigger?

A: An external trigger is a signal outside the Logic Analyzer, which is used for the simultaneous test of 2 test tools. For example, the Logic Analyzer can be started by one signal from another test tool. Or when it is triggered, it can output one signal to another test tool. The Logic Analyzer is often used for triggering an oscilloscope.

TI10. Why does Double Mode not coincide with Signal Filter Delay?

A: In order to set out the perfect waveform from the Logic Analyzer and achieve optimal memory efficiency, you can use the **Signal Filter** when using **Double Mode**; the system doesn't support the function of **Filter Delay**.

TI11. How do I update my software?

A: The software will automatically check for and download updates. This function deletes old software first and then downloads and installs the latest version.

6.5 Others

OT01. How was the Logic Analyzer developed?

A: It took us more than two years to develop this product. We envision "Everyone carrying the Logic Analyzer," and we would like to make some contributions to the electronics industry in return. We also wished to transform the stereotypical OEM factory into a world class R&D center.

OT02. Why is there a rich information database for game chips rather than the Logic Analyzer?

A: First of all, we apologize for any inconvenience caused by the lack of information pertaining to Logic Analyzers. We are currently working very hard on multilingual information and documentations pertaining to the Logic Analyzer. Visit our website for the latest drivers, software, and manuals:
http://www.zeroplus.com.tw/new_instrument/index.php?lang=eng.
In the meantime, we will have updates ready when verified error free.

OT03. What was the original intention of developing this item?

A: Originally, the Logic Analyzer was just for use by our engineering department. Later on, we saw the greater need for this kind of devices. We made numerous enhancements and made it available to the public.

Conclusion

This chapter is full of hard facts for engineers. The contents of this version of the User Manual may look more different than the one on the web. Every engineer finds new problems, new solutions, or other issues, during real life applications. Though there are dozens of questions here, we look forward to your feedback, which is important for future versions. It may help us produce more efficient and accurate devices so that we will offer you much better service.

7 Appendix

7.1 Hot Keys
7.2 Contract Us

Objective

In this chapter, users will learn the functions of all defined Hot Keys in the software interface of the Logic Analyzer.

7.1 Hot Keys

Table 7-1: Hot Keys (1)

Hot Key	Equivalent Orders	Statement
A	Go to A Bar	Move the A-bar to the center of the waveform area; select A-bar by the cursor.
B	Go to B Bar	Move the B-bar to the center of the waveform area; select B-bar by the cursor.
T	Go to T Bar	Move the T-bar to the center of the waveform area; select T-bar by the cursor.
E	Change to Enclose mode	Change the mouse mode to Enclose.
H	Change to Hand mode	Change the mouse mode to Hand.

Table 7-2 : Hot Keys (2)

Hot Key	Equivalent Orders	Statement
Ctrl + A	Go to A Bar	Center A-bar.
Ctrl + B	Go to B Bar	Center B-bar.
Ctrl + C	File -> Graph	Open Capture Graph dialog box.
Ctrl + E	Data ->Enclose	Change Mouse mode to Enclose mode.
Ctrl + F	Data -> Find Data Value	Search specific data with predetermined conditions.
Ctrl + G	Bus/Signal -> Group into Bus	Group selected signals into a Bus.
Ctrl + N	File -> New	Create a new file.
Ctrl + O	File -> Open	Open a saved file.
Ctrl + P	File -> Print	Print an active file.
Ctrl + S	File-> Save	Save an active file with its current name, location and file format.
Ctrl + U	Bus/Signal -> Ungroup from Bus	Ungroup signals (Pins) from a Bus.
Ctrl + Z	Data -> Undo Last Zoom	Reverse the last zoom.
Ctrl + Shift + E	File->Export	Open the Export dialog box.

Table 7-3 : Hot Keys (3)

Hot Key	Equivalent Orders	Statement
Page Down	Operate the position shown	Go to next page of the data or the waveform.
Page Up	Operate the position shown	Go to prior page of the data or the waveform.
Home	Operate the position shown	Go to the beginning of the data or the waveform.
End	Operate the position shown	Go to the end of the data or the waveform.
Up	Operate the position shown	Move the cursor up a grid.
Down	Operate the position shown	Move the cursor down a grid.
Left	Operate the position shown	Move the selected Bar or display left to the prior waveform or data.
Right	Operate the position shown	Move the selected Bar or display right to the posterior waveform or data.
ESC	Operate the position shown	Release all selected bars, and changes Mouse mode to Normal.
Space	Change the trigger conditions	Change trigger conditions.

Table 7-4 : Hot Keys (4)

Hot Key	Equivalent Orders	Statement
F1	Help -> Logic Analyzer Help	Logic Analyzer Help
F2	Decrease the sampling rate	Decrease the sampling rate.
F3	Increase the sampling rate	Increase the sampling rate.
F5	Run/Stop -> Single Run	Execute the acquirement once.
F6	Run/Stop -> Repetitive Run	Execute the acquirement continuously.
F7	Run/Stop -> Stop	Stop acquiring data.
F8	Data -> Zoom Out	Zoom out the waveform.
F9	Data -> Zoom In	Zoom in the waveform.
F11	Data -> Before	Move forward to the prior variation waveform and center that location.
F12	Data -> After	Move forward to the next variation waveform and center that location.

7.2 Contact Us

Table 7-5: Contact Us

Contact Us	
Copyright 1997-2009, ZEROPLUS TECHNOLOGY CO., LTD	
Headquarter	
Taiwan-Chung Ho City	ZEROLUS TECHNOLOGY CO., LTD. 3F., No.121, Jian Ba Rd., Chung Ho City, Taipei County, R.O.C. Tel: +886-2-6620-2225 Fax: +886-2-6620-2226 ZIP Code: 23585
Instrument Division/ Business Department	
Taiwan-Hsinchu City	ZEROLUS TECHNOLOGY CO., LTD. 2F., No.242-1, Nanya St., North Dist., Hsinchu City 30052, Taiwan (R.O.C.) Tel: +886-3-542-6637Fax :+886-3-542-4917 ZIP Code: 30052 E-Mail: hunter@zeroplus.com.tw
Taiwan-Chung Ho City	ZEROLUS TECHNOLOGY CO., LTD. Address: 2F, NO.123, Jian Ba Rd, Chung Ho City, Taipei Hsian, R.O.C. Tel: 886-2-6620-2225 Ext.:200 Fax: 886-2-6620-2226
Other Service Departments	
China-Shenzhen	ZEROPLUS TECHNOLOGY (DONG GUAN) CO., LTD. Room 2821, B2 Section, Building 1, Hong Rong Square, District 80, Bao'an, Shenzhen City, Guangdong Province, China Mainland Tel: +86-755-2955-6305~6 Fax: +86-755-2955-6306 #808 ZIP Code: 518102
China-Shanghai	ZEROPLUS TECHNOLOGY (DONG GUAN) CO., LTD. 101, No. 172, Alley 377, Chen Hui Road, Zhang Jiang, Pudong New Area, Shanghai City Tel: +86-21-50278005~6 Fax::+86-21-50278006 ZIP Code: 201203

Users can download the newest Software and User Manual.

ZEROPLUS is the brand of ZEROPLUS TECHNOLOGY CO., LTD.

The other brands and products are the brand or registered trade mark of the individual company or organization.

Conclusion

The demonstrations in this User Manual will enhance users' understanding of our products in future issues, even though the manual ends here. We thank you for choosing the Logic Analyzer. Please contact us if you feel anything that could be done better, either in software or hardware. We appreciate your feedback.